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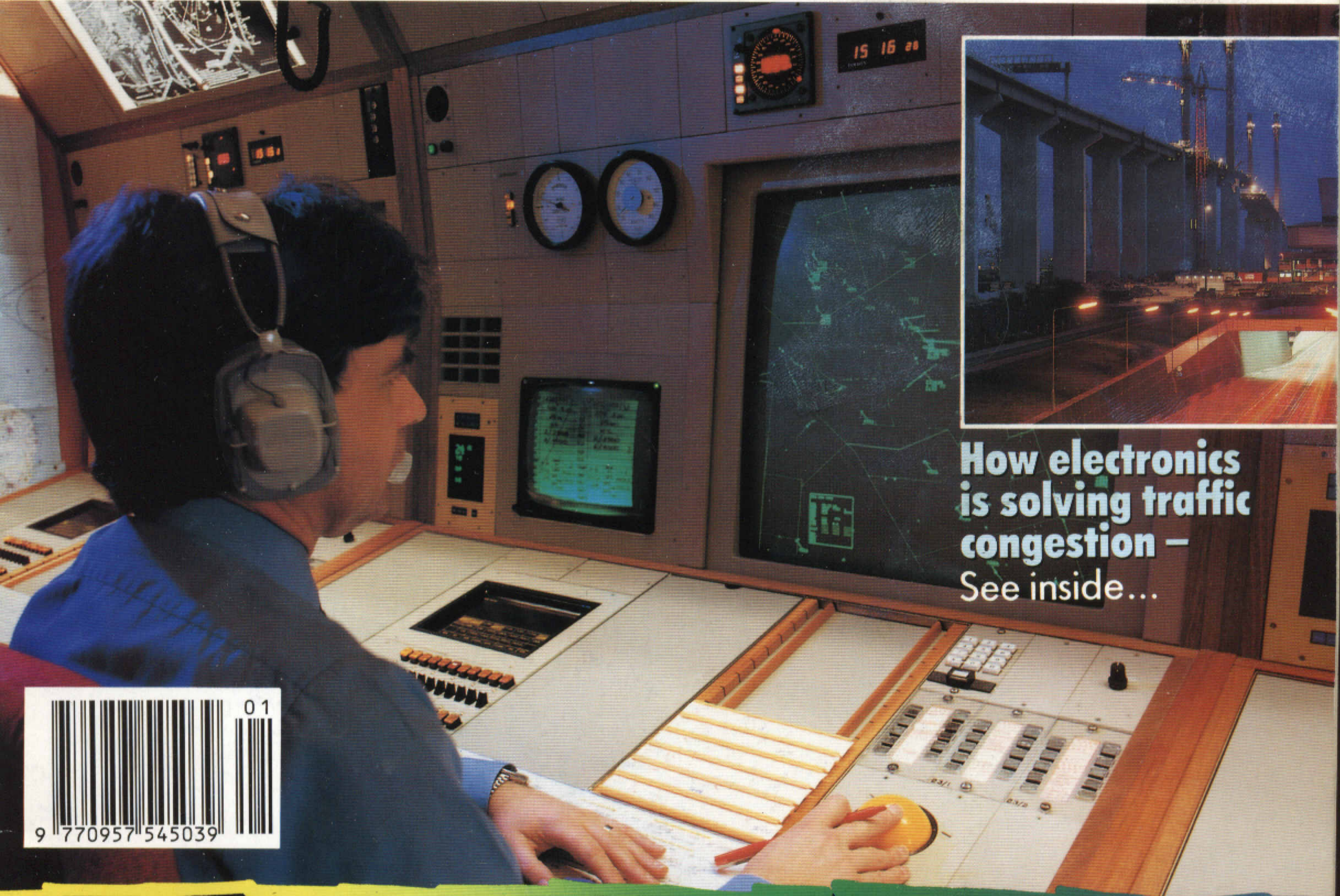
BRITAIN'S BEST SELLING ELECTRONICS MAGAZINE

No. 49

ELECTRONICS
The Maplin Magazine

JANUARY 1992 · £1.60



How electronics is solving traffic congestion – See inside...

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* Overcome signal transmission problems with a Direct Inject Box
* Find out how electronic engine management and ABS works
* Discover the importance of electronic systems in aircraft
* Protect your bicycle with an easy-to-build alarm unit
* Win a visit to the Capital Radio Studios in London

PLUS! How to... Connect computers without wires, Design DC power supplies, Understand digital logic, Build an analogue reverberation unit, and much, much more!

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CONTENTS

JANUARY 1992 VOL.11 No.49

EDITORIAL

Happy New Year, and a very warm welcome to another issue of 'Electronics'. Being the first issue of the new year, it seems appropriate there are three new serials starting this issue: Electronics in Aviation, the Design and Application of Sequential Logic and an Introduction to Boolean Algebra. The latter two, both written by Graham Dixey, run concurrently and are closely allied to the same subject – that of digital electronics. Often, a circuit diagram containing a proliferation of logic gates confuses both the engineer and the electronics hobbyist alike; this need not be the case. The aim of the series on sequential logic is to not only explain *how and why*, but to also show the way in which logic circuits may be designed and applied to fulfil a particular need. To enable the designer to provide the best solution to a particular 'logic problem' it is necessary to employ boolean algebra. By using this branch of mathematics it is possible to find the most practical and economic means almost entirely on paper, before progressing to a physical prototype. If it has been a long while since you learnt about digital logic and boolean algebra, then this will be just the kind of revision to blow away the cobwebs!
There is of course a complete line-up of projects, features and regulars, but I'll leave you to read and digest them yourself. So until next month, I hope that you enjoy reading this issue as much as the 'team' and I have enjoyed putting it together for you!

R Ball

ABC 33,837

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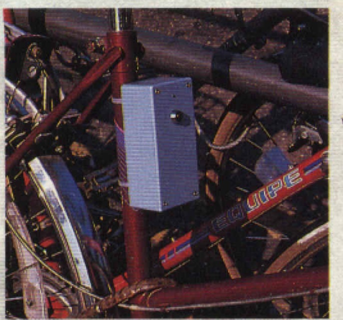
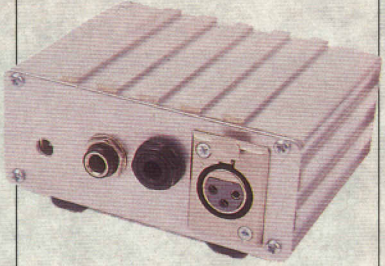
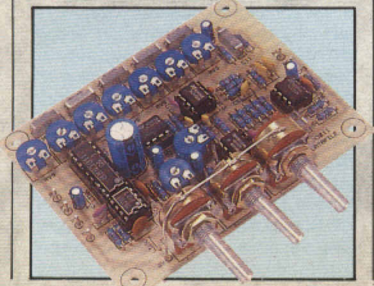
Published by Maplin Electronics Plc.
Colour Separations Stirling Graphics Ltd., 16-22 West Street, Southend, Essex SS2 6HJ.
Printed by Severn Valley Press, Caerphilly, Mid Glam. CF8 3SU.
Distributed by United Magazine Distribution Ltd., 1-11 Benwell Rd, London N7 7AX.
Mail Order P.O. Box 3, Rayleigh, Essex SS6 8LR.
Retail Sales: (0702) 554161. **Retail Enquiries:** (0702) 552911. **Trade Sales:** (0702) 554171.
Cashtel: (MODEM) (0702) 552941.
General: (0702) 554155.
Fax: (0702) 553935. **Telex:** 995695.

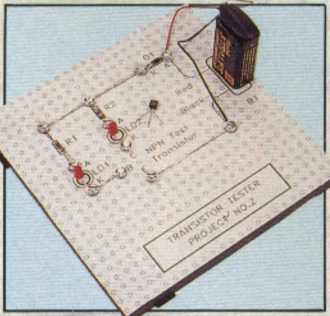
Cover Picture: Siemens Plessey 2000 line Radar display unit, installed at Manchester Airport.

PROJECTS









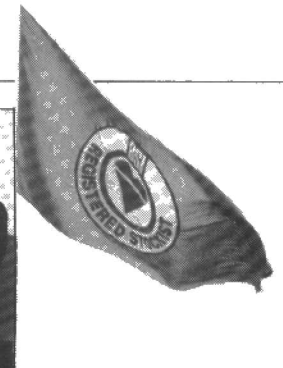
FEATURES

REGULARS

Prices shown in this issue include VAT at 17.5% (except items marked NV which are rated at 0%) and are valid between 6th December 1991 and 31st December 1991.

NEWS Report

Maplin Flies the Kite



Maplin has been awarded the British Standards Institute BS5750 Quality Assurance Certificate – the famous 'Kite' mark. To mark the occasion, David Trippier, Minister for the Environment and Countryside, paid a visit to the new Maplin Distribution Centre in Wombwell, near Barnsley in South Yorkshire. In making the official presentation, the Minister congratulated the company on its achievement. "The Award", he said, "marks a significant milestone in the fortunes of Maplin. Quality ensures that goods don't come back, but customers do."

Replying, Roger Allen, Managing Director of Maplin, said that increasingly, customers are demanding BS5750 quality standard products. "The already high quality of Maplin products will be enhanced by the Certificate – the culmination of extensive assessment by the BSI Quality Assurance team. The way to success for companies in the electronics business is to establish firm quality standards and this is exactly what Maplin has achieved." Roger also took the opportunity to thank local authorities and councils for their assistance in granting planning approvals and controls.

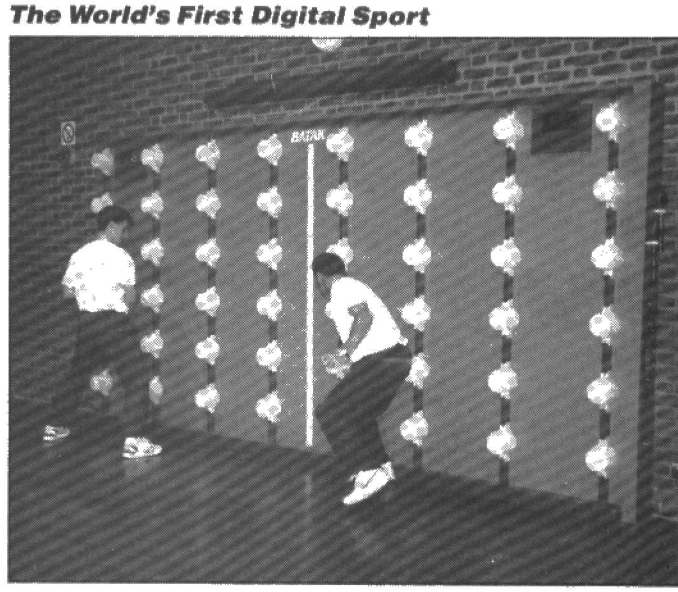
To further mark the event, David Trippier, together with Wombwell chief executive, Lewis Bowman, hoisted the BSI flag over the complex.

Learning to be Secure – with Maplin

Pupils from the Cornelius Vermuyden School, Canvey Island, Essex, stole the prize in a schools competition organised by PC Gordon Sinclair of Essex Police. Entrants had to conceive ideas that would promote the force's Crime Prevention scheme, grabbing the attention of the general public (and hopefully not running away with it!) The winning entry took the form of posters submitted by four of the school's pupils. Crime prevention officer Superintendent Iain Munro and his colleagues selected one of the four – that designed by Clint Nagi – to win a special prize, donated by Maplin. In addition to this prize, which was a Road Winner radio-controlled car, Maplin also presented a £400 burglar alarm to the school. This was gratefully accepted by Ron Grant, head of the school's Information Technology unit, who helped to design and print the posters.

Making off with the prizes: from left to right; Bob Kirsch, Maplin's technical services manager; Ron Grant; Clint Nagi and Supt. Iain Munro, holding Clint's poster.

The World's First Digital Sport



Described as the world's largest physically interactive computer controlled game, the equipment, called Batak, is a new sport for the Nineties. With it you can play squash or almost any active ball game without a ball, without an opponent and without even having to go onto a court. Play is against a wall which incorporates electronically-activated targets which light up when hit by a foam tipped racket. Batak comprises 48 translucent targets in rows of 6 to 8 aluminium uprights which are fixed to the vertical playing surface. The computer controls the sequence and speed of target illumination, gives audio responses for 'strokes' and 'misses' and times and scores the game on two large LED readouts mounted on the 'playing interface'.

The computer based technology enables an infinite number of different games to be played at varying speed/skill levels according to age and fitness. Custom programmes can be created for training, warm-up sessions, therapeutic, aerobics and weight loss purposes. Already there are three machines being play tested, one at Bisham Abbey, one at Copthorne Club and one in Japan. Details, Tel: Batak Ltd. (0293) 785132.

BT Suffering from PIN-Prick

It is a quiet news front for BT this issue. The corporation has announced it is splitting its present premium rate service into two. General interest and family entertainment services will be moved to a '0891' prefix, while '0898' will continue to be the 'adult services' number. It could be, of course, that BT has got its collective head down, investigating a security nightmare revealed by the publication TRR. It seems that BT encourages its 800,000 charge-card customers to use their cards when making calls from a client's telephone. They simply dial 144, then key in their card number and PIN, followed by the phone number they want to speak to. This means that the host office does not have to pay for the call – it is charged to the cardholder's account instead. Wonderful idea in theory.

But in practice, if the host's telephone is connected to a call logging device, a very serious breach of security can arise. Most call loggers will, apparently, faithfully record exactly what is dialled – including that all-secret PIN! Later a neat printout, showing the card charge number and PIN, will be produced. Should the card be abused, BT will argue that the cardholder must have revealed the PIN, and he must therefore bear the full cost of the abuse. According to TRR, BT have no intention of warning cardholders of the possibility of call-logger abuse at present. Details, Tel: TRR (071) 274 8725.

Enter Berni the Rabbit

Despite all this high tech activity, Philips still has time (and the funds) to be a sponsor for two of the world's major soccer championships – the 15th World Cup, which will be held in the USA during June and July 1994, and the European Championship in Sweden in June 1992. Berni, the rabbit created by Walt Disney, and who is the official mascot of the European Championship, will be used in all Philips' promotional material to display the company's status as official sponsor of the event.

QEII Bridge Opening

There were no complex microcircuits to impair the opening of the new Queen Elizabeth II Bridge. The third crossing from Thurrock, Essex, to Dartford, Kent, was opened by Her Majesty The Queen on 30th October 1991 and Maplin was there.

The bridge, within minutes of The Queen opening it to traffic, immediately increased the capacity at this notorious part of the M25, to 150,000 vehicles per day. This cable-stay bridge, the largest of its type in Europe, is a wonderful feat of engineering, and also features Automatic Vehicle Identification – an electronic means of speeding up the toll collection. It was built in a little under three years at cost of less than £100m, even after allowing for the purchase of the existing tunnels.

The design has not been without its critics, particularly in the area of height – over 200ft from the river, and wind vunerability. As one of the first travellers on the Bridge, wind did not present a problem to us and as far as the height, a lot of that is compensated for by the view!

Maplin are proud to have been part of the opening, and be able to present a full report on the bridge and the operation of the electronic toll collection system, see page 16 of this issue.

Its a Cracker!

Seven years ago Band Aid caused a revolution. Bob Geldof and friends proved to a watching world that there were new and imaginative ways of tackling the issues of global poverty and challenging the public to give generously.

Over the past couple of years, Christmas Cracker Trust have organised fund-raising projects all over Britain, in fact you may well remember the 'Christmas Cracker' restaurants in many local high streets last Christmas. The funds raised have and still are being used to help bring fresh water supplies to people in India. Both the Prime Minister, John Major, and the Archbishop of Canterbury, George Carey, have given encouragement to the projects.

Enter 'Radio Cracker' – a project launched by Christmas Cracker Trust, organised by Alpha Magazine and Oasis Trust, and sponsored by Tear Fund – set to once again bring people's attention to world issues. Recent changes in broadcasting legislation has enabled a country-wide chain of Radio Cracker community radio stations to be set up in conjunction with the Radio Authority and the Department of Trade and Industry. The stations are broadcasting under Special Event Radio licences, which, in the words of the DTI "is a Radio Service restricted in duration and geographical coverage, using a low powered, freely radiating transmitter, broadcasting for reception on normal radio receivers."

During the period 30th November to 24th December 1991, money will be raised for deprived children and young people around the world, by asking local shoppers and residents to request songs and dedications in return for donations. Radiophonic stunts, competitions, auctions and the sale of advertising will help to bring in funds to be dispersed by Churches and Christian agencies, such as Tear Fund, working in the developing world.

On a local basis Maplin has helped the Southend Radio Cracker station by supplying an answer-phone; cable, components and modules to build the all important audio mixing desk; and giving technical assistance. Nationally, regional Maplin stores have been a useful port of call for the technical teams involved in setting up the stations; supplying components and advice. In the near future 'Electronics' will report on just how the Radio Cracker stations got on!

For details of where to find your local Radio Cracker station on the FM dial, check local press, or Tel: 021-773-9333, for details.

Half a Dozen CD Photo-Sized Prints Please

Photos of a CD technology kind are to be marketed in Europe this summer by Philips. The Photo CD system allows consumers to take pictures as they normally would using 35mm cameras and colour negatives or slide films. When they take their film in for processing, they will have the option of ordering a Photo CD in addition to the prints and negatives they normally receive.

Cable Wars

Government watch-dog Sir Bryan Carsberg of OFTEL, apparently none the worse for bruising attacks made on him by the industry following his indecision over BT connectivity, has turned his attention to the cable operators. Unless they get their act together in providing local services, he warns, he will take drastic action. Where one locål contractor is making rapid cabling progress, he will consider extending that cable company's franchise across previously negotiated boundaries, revoking, if necessary, licenses. No doubt the cabling industry expect OFTEL to change its mind on this matter also.

Certainly, on speaking at a PA Consulting Group conference, Videotron called the present government's 'milestone' building targets 'suspicious'. Multiple system cable operators, he said, should be allowed to concentrate their investment on building home systems in whatever geographical focus that business objectives dictated. Similarly, the authorities should be encouraging the mix of cable television and cable telephony which would serve to maximise the return on capital.

Meanwhile, a survey conducted by the Independent Television Commission reports that broadband cable franchisees have now built their systems past the one million homes mark. The number of homes connected to those systems on July 1991 was nearly 200,000, an increase of 80% over the previous year. If you are keen to receive cable services, the most active area is Croydon, which has some 23,000 connections, followed by Swindon, Windsor and Northampton. Bottom of the connections list are Liverpool, Camden and East Lancashire. When it comes to the choosing of programme channels watched on cable, Sky One leads the field. Next comes Sky News, then Sky Sports. Surprisingly, the 'in-the-news news channel', CNN, comes near the bottom of the watching list.

On the basis that what the US does today, the UK will follow tomorrow – or the day after – a Frost and Sullivan Report suggests that your television could soon be ringing as often as the phone. Cable TV is not just for entertainment anymore; it is installing hardware costing almost $1·6 billion annually and is on the way to becoming an interactive communications network. The basic US idea is that cable companies will compete with telephone companies and others to provide an array of services over the 'networks' they already have in place, but which are utilised for carrying entertainment.

PICTURE CAPTION CHALLENGE

Just who is the rugged looking individual pictured above and what is he up to?

- ★ Is he a maintaining a SCUD watch off the Iraqi coast.
- ★ Calling in extra supplies of BT petrol from a Tesco forecourt.
- ★ Prompting The Royal Shakespeare Company at the Barbican.

Give up? Well Cellnet have launched a marine information service to meet the safety needs of their business customers who take part in water sports during their leisure hours and take their mobile phones with them. Bet you would never have guessed.

What's On and Where

4–6 December. European Satellite Communications, QE2 Centre, London. Tel: (081) 868 4466.

5–8 December. Computer Shopper Show, Wembley. Tel: (081) 868 4466.

2–5 January 1992. Holiday and Travel Fair, NEC, Birmingham. Tel: (081) 948 9900.

Open until 19 January 1992. Doctor Who has extended his travel through time and will be appearing over Christmas and the New Year. Museum of the Moving Image, South Bank, London. Tel: (071) 928 3232.

Open until 19 January 1992. Michael Faraday 1791–1867 National Portrait Gallery, London. Tel: (071) 306 0055.

Open until 19 January 1992. Japan's National Space Development Agency, Science Museum, London. Tel: (071) 938 8000.

4–6 February. Portable Computer Communications Show, Wembley, Middlesex. Tel: (071) 383 3323.

23 February. Northern Cross Radio Rally, Rodillian School, on the A61. (GOFLX). Tel: (0532) 827883.

Please send details of events for the Diary Listings to The Diary Editor, 'Electronics'.

ELECTRONICS IN AVIATION

Part One
The Early Years

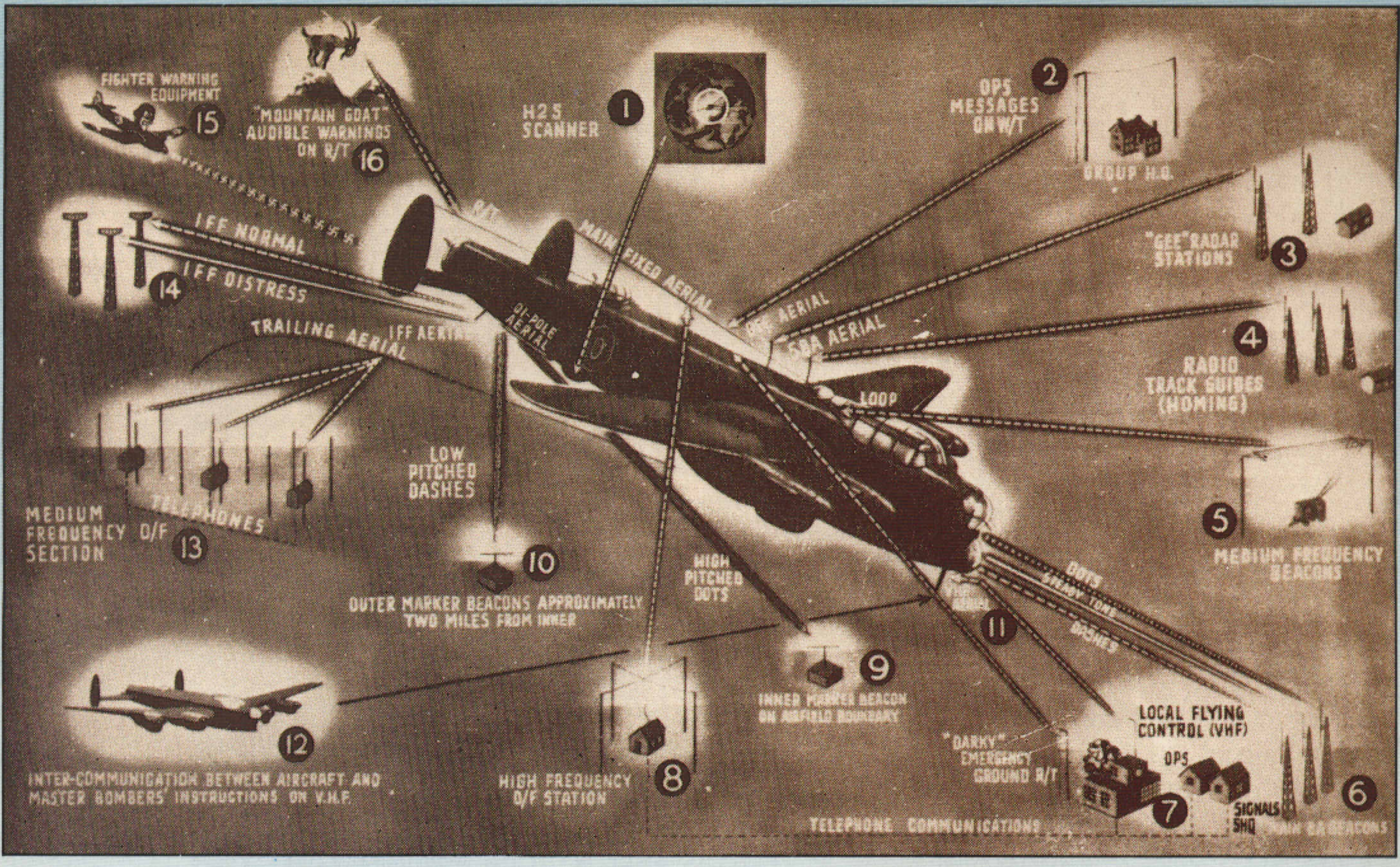
by Chris Yates

It may come as something of a surprise to the casual observer, that the origins of aviation go back way beyond those heady days when Orville and Wilbur Wright first took to the skies in an aeroplane. In fact, the principles of heavier-than-air flight owe more to British ingenuity than American industrial might, thanks to the vision of baronet, Sir George Caley. With his research in 1799, into the problems and principles of flight, he was many years ahead of his time. Despite that, he mastered the art, and by 1809 was able to demonstrate his theories by building the world's first model glider. Today he is acknowledged as the founding father of the science of aeronautics. His discoveries not only aided man to conquer the skies, but also the heavens as well. Predictably, the scientific community of the time took little heed of his theories, and the world had to wait another century before the Wright brothers continued his work.

It was 17th December 1903 when Orville Wright, flying from Kitty Hawk – a remote spot on the Atlantic coast-line of North Carolina – entered the history books as the first man to experience powered flight. He was airborne for all of twelve seconds, but that momentous occassion signalled the dawning of a new era. An age when man could cross oceans and continents by air, and reach for the moon and stars.

Pioneering Days

The early years of aviation owe more to mechanical than electrical or electronic engineering, and it wasn't until 1912 that the first piece of electronic hardware – a radio set – was airborne. At the time, 'wireless' was much in its infancy, and stealing a march on the rest of the world, it was the Americans who discovered its value to aviation. Flying over New York State, the new fangled trans-ceivers (transmitter/receivers) were used to pass vital airfield weather information – data as important today as it was then. In that same year, a British army pilot became the first to see artillery fire from the air, which prompted the authorities



to kit out some aircraft with morse transmitters and cameras. However, despite these early successes, the Great War came and went with many an allied aircraft having to land before the 'spotter' could send his report to headquarters.

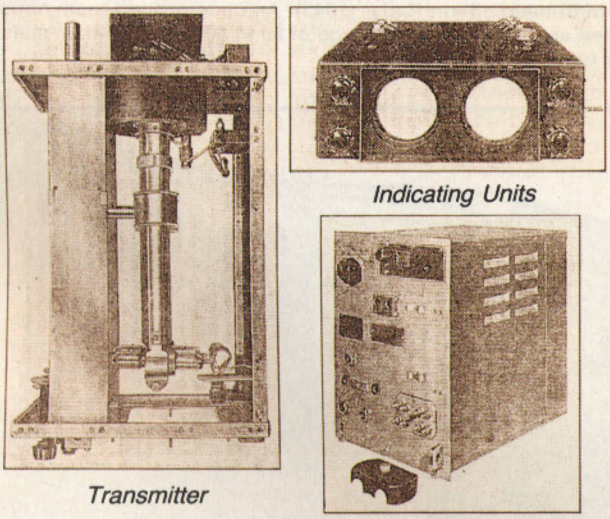
Direction-Finding and Radar

By contrast, the post-war years were a time of great advancement for both aviation and electronics in aviation. Not only did the first-atlantic and polar ice-cap flights take place, but the jet engine was first mooted and Radar became a reality.

Radar was a natural progression from radio, and through the work of Sir Robert Watson-Watt, has its origins back in the midst of war. Sir Robert joined the Meteorological Office in 1915, and began work on the detection and locating of thunderstorms. By then it was known that such storms were both a threat to the fragile aircraft of the day, and a prolific source of atmospheric noise. Through his studies he developed a simple radio direction-finder which gave their general position, but it was not until 1922 and the advent of the cathode ray tube that he could see such storms and predict their direction of activity.

Using the CRT to study the ionosphere with the aid of distance radio signals, Watson-Watt discovered he could measure its distance by timing returns, and became convinced that the principle could also be applied to aircraft in flight. Persuading the Air Ministry that the idea had some merit, 1935 saw £10,000 made available and work started on the world's first radar station at Orfordness in Suffolk.

Top: Radio and radar equipment of a war-time aircraft. 1) H2S Ground Radar. 2) Radio communications. 3) Long range 'Gee' radar navigation system. 4) Standard Beam Approach guides aircraft to airports. 5) Radio beacons. 6) Main Beam Approach helps pilot maintain correct approach path. 7), 8), 11) HF direction-finding aerials and VHF equipment for local Flying Control. 12) VHF air-to-air communications. 13) MF direction-finding stations. 14) IFF radar system. 15) Attack warning radar identifies aerial attack. 16) 'Mountain Goat' radio beacons to warn navigators of high ground, cliffs and mountains.



Indicating Units

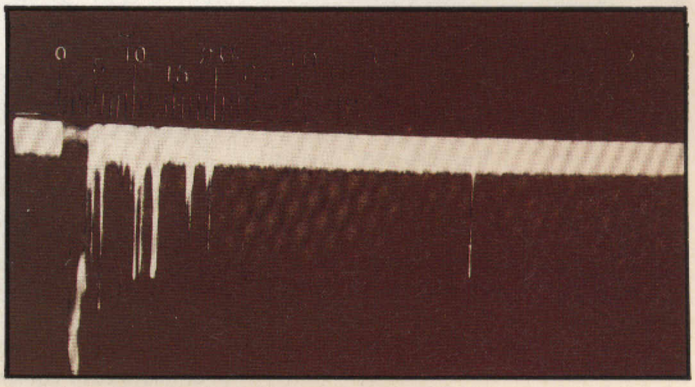
Transmitter

Modulator

Above: AI Mk IV Radar (1941–1945). The first operational night fighter radar for which EMI produced the modulator (to A. D. Blumlein's design) and GEC produced the transmitter working in conjunction with EMI. Approx. 8000 systems were produced. Split receiving dipoles on the wings for azimuth and elevation angle measurements.

Left: A Bristol Beaufighter fitted with the AI Mk IV Radar for night interceptions.

Below: Type A Range Display. The vertical spikes indicate radar reflections from various objects. The rule above is graduated in miles. The radar echoes seen from 0 to 20 miles are from nearby masts, towers and hills, and are known as permanent echoes (PE's). A live response from an aircraft 52 miles away can be clearly seen.



Success was almost immediate, and by June of that year, Watson-Watt and his team were monitoring the movement of flying boats operating from the Felixstowe Air Station.

Identification Friend or Foe

Whilst it was all well and good to be able to follow the progress of aircraft in flight, some thought had to be given to identifying them – thus Identification Friend or Foe (IFF) was born. The system was stunning in its simplicity. Consisting of nothing more than a receiver which amplified the incoming radar transmission, added a coded signal and returned it to the ground – IFF saved many World War II pilots from being shot down by friendly fire. IFF was the forerunner of the transponders of today. These modern sets can inform ground controllers of an aircraft's call-sign, altitude and heading.

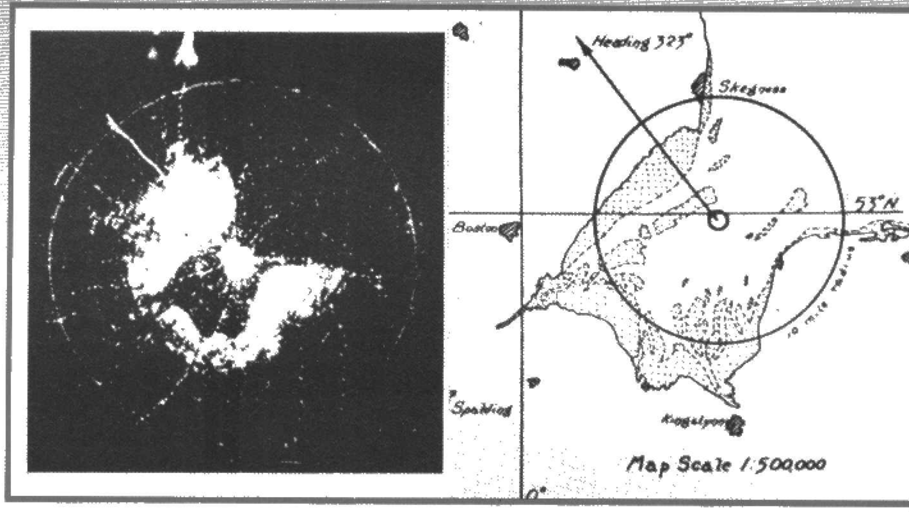
International Aviation

Whilst the scientific work forged ahead – often into new untried technology – the fledgling airlines of the day began to cast their tentacles far and wide. The first daily international passenger service got off to a flying start on the 25th March 1919 when a de Havilland 4a of Air Transport and Travel took off from Hounslow for its 2½ hour flight to Le Bourget near Paris. On board were one passenger, several pots of Devonshire cream, a brace of grouse and newspapers. It was the start of an aviation war which is still going on today!

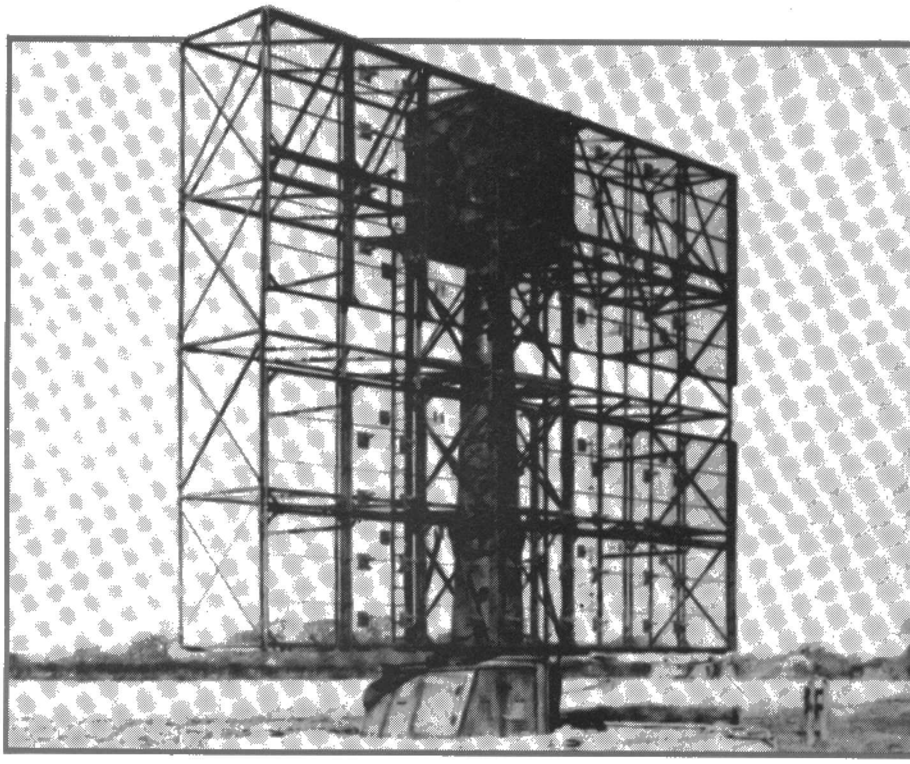
From the outset of scheduled international passenger services, the British Government had its heart set on linking the Empire by air – thus Imperial Airways, the country's first nationalised airline, was formed in 1924. Imperial was Britain's flag carrier, an instrument of foreign policy. The coming years saw its DH66 Hercules, Armstrong Whitworth Argosy and Handly Page 42 aircraft reaching out to the far-flung corners of the globe. At the same time our American cousins were looking to expand their influence in Europe, but it wasn't until 1937 that Pan American and Imperial started reciprocal services across the Atlantic. These exciting times came to a grinding halt in September 1939. War had returned to Europe, and as a result international air travel was suspended for the duration.

World War II

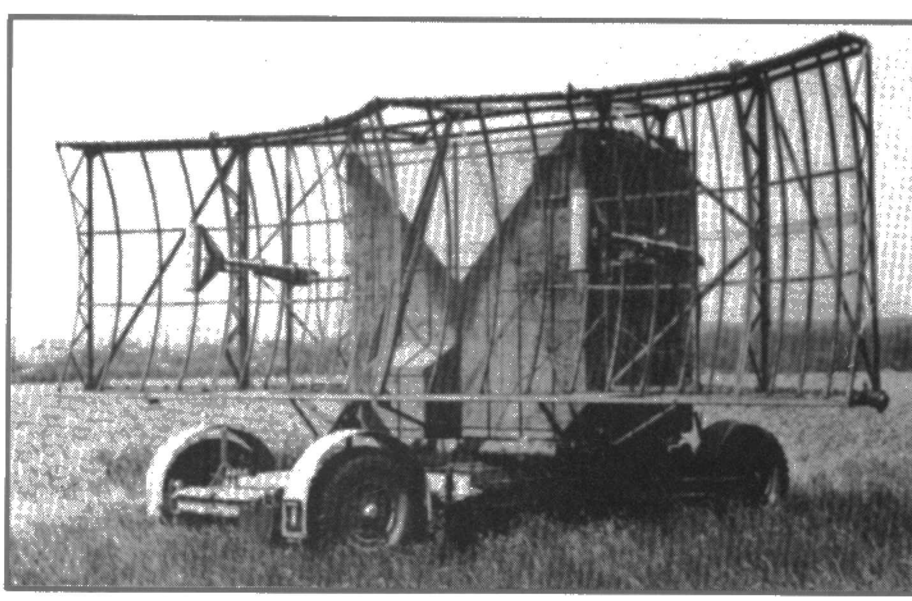
Whilst many of the pre-war civilian aircraft found themselves pressed into military service, so too did Watson-Watts radar experiments. By this time the east coast was protected by a chain of radar stations which could 'see' aircraft to a range in excess of 150 miles – it became the backbone of Britain's air de-



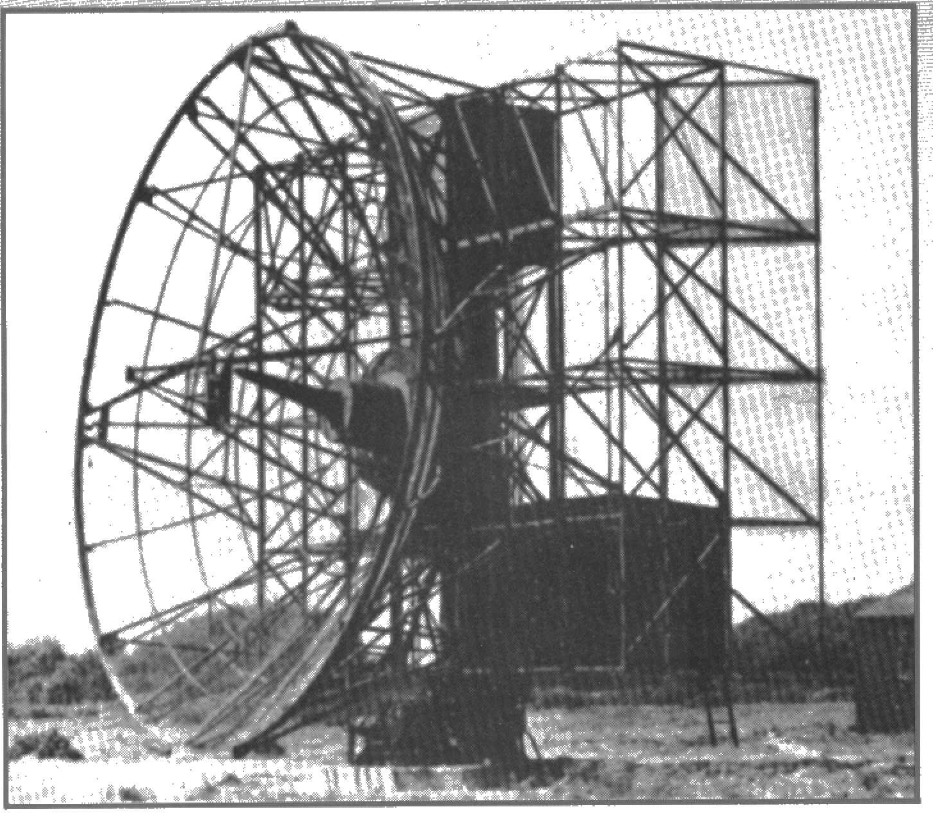
H2S Radar screen and true map, photograph shows a radar map of the ground beneath an aircraft. The map allows a comparison to be made against the radar image.



AMES Type 7 Ground Control of Interception Radar (1943). An underground room housed the transmitter and associated equipment. Typical range of 80 to 100 miles with an altitude of 60,000ft and elevation up to 40°.



AMES Type 11 Portable Fighter Direction Radar. Wavelength: 50 to 60cm. Range 100 miles. Update period: 20 seconds. Used for air surveillance at low altitude prior to the introduction of microwave equipment.



AMES Type 16 long range Fighter Direction Radar (1944–1945). Wavelength: 50 to 60cm. Range: 130 miles. Rotational speed: 3RPM. Elevation scan: 10°. Dish diameter: 30ft. The usual technique was to scan a 90° sector at 3RPM and speed up over the remaining 270° to give an update period of approx. 10 seconds. Elevation coverage: +2° to +12°. Usually used with AMES Type 12 (vertical nodding height finding radar).

fences. In conjunction with the now de-rigour two-way radio facilities, radar was used to direct fighters in flight, and was the secret weapon behind allied success in the Battle of Britain.

The technology behind these radar stations had, by this time, moved into the realms of the unknown. After the early experiments with 6MHz sets, the next four years saw advance after advance until a limit was reached at 200MHz. This was the maximum usable frequency at which great power could be generated, and became the operating standard for airborne, seaborne and ground based radar, until the invention of the resonant Magnetron in 1940.

The Magnetron

The magnetron was an amazing discovery which – with the aid of plan position indicator displays – was to revolutionise radar with its ability to produce 15kW of RF energy at frequencies in the Gigahertz range. For the first time pictorial representation of amazing clarity could be produced, and it provided the benchmark for RAF radar until 1957.

Testing Times

Both radio and radar received their baptism of fire during the final years of the war, thanks – in part – to the massed bombing raids over Germany's major cities. With so many aircraft flying in such tight formations the scene was set for an aviation disaster, but it did not happen due to the birth of Air-Traffic Control (ATC). With their 'radar eyes' looking skyward, ground controllers could now see aircraft in flight even though their pilots often could not see one-another. Using procedures similar to those of today, it was possible to physically separate aircraft by radioing instructions to their pilots.

Home to Mother

Whist radio and radar played a dual role in World War II, so did the spin-offs of which aviation today benefits. One of the earliest was affectionately known as 'Mother'. This was an IFF type device which allowed aircraft to interrogate it to obtain range and bearing to home base. It is responsible for saving many lives, and the Distance Measuring Equipment (DME) of today is derived from it. Another spin-off which has stood the test of time is the LORAN long-range navigation system. Based upon a network of high power, low frequency transmitting stations, LORAN can be used to fix an aircraft's position to within one nautical mile anywhere in the world.

At the same time cockpit instrumentation started to move from mechanical to electronic, through experimentation with the radio altimeter, and developments in marker beacon technology allowed the air routes to be laid out. Of course some element of control had to be exercised over these routes, and the ATC lessons of the bomber raids led to the network of air-traffic control systems we have today.

High Tech

By the end of the war aviation technology was moving at a rapid pace. Although Air Commodore Sir Frank Whittle had patented the jet engine in 1930, it was not until after 1945 that Britain got its first jet fighters.

Again the seeds for revolution were sown, and the technology took the aviation world by storm. Meteors, Shooting Stars and a lone Messerschmitt were amongst the first flying examples, but civil aviation didn't take long to catch on. Maintaining its lead on world aviation the British aircraft industry produced the first two jet airliners – the turboprop Vickers Viscount and the infamous de Havilland Comet. They spurred an explosion of air travel, and to meet these needs, not only the science of aeronautics but also ATC in its many forms had to grow with it. Controlling the skies was a matter of upmost importance, and with a network of new VHF communications and microwave radar stations, by the late fifties Britain was once again a world leader – this time for air safety.

Of course, in the intervening years technology has once again taken great leaps forward, and in the coming months we will be taking a close look at the world of aviation, and the increasingly vital role which electronics play.

Terminology

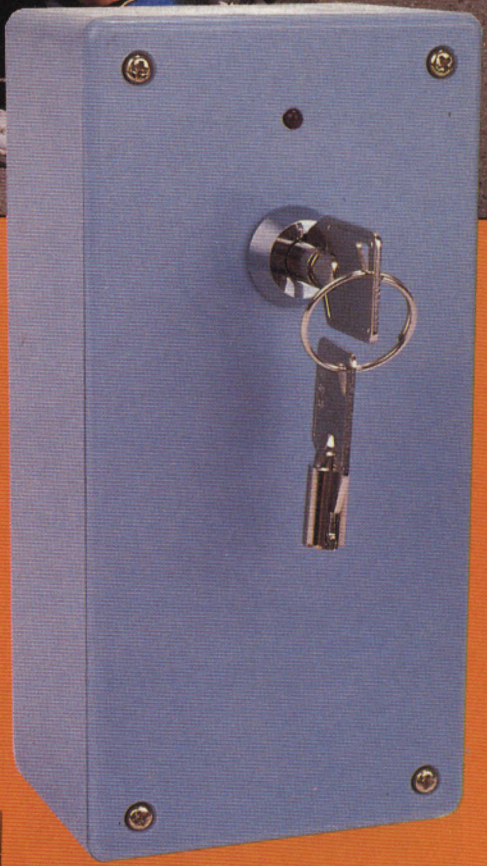
Term	Meaning
CRT	Cathode-Ray Tube
IFF	Identification Friend or Foe. A means of interrogating an aircraft by Radar.
Transponder	The modern equivalent of IFF. This allows ground controllers to interrogate modern jetliners to find out their altitude, heading and call-sign.
DME	Distance Measuring Equipment.
LORAN	Long Range Navigation System, based upon a worldwide network of high power, low frequency pulsed radio transmitters.
Resonant Magnetron	A diode with a cathode and anode in a cylindrical package. The anode is spilt into two parts, and comprises multiple cavities which resonate at the operating frequency. The device is mounted in a powerful magnetic field.

Vibration Cycle Alarm

by Dave Goodman

FEATURES

★ Loud sounder with 2 minute time-out ★ Vibration and movement sensing ★ 'Warning' and 'anti-tamper' switch facilities ★ Keyswitch arming delay



The completed Cycle Alarm.

The number of times I have seen bicycles left unattended (and unlocked!) in the streets or propped up against newsagent shops I could not start to recall, although I do remember having my own bike stolen in such a situation some years ago. To make matters worse, expensive custom-designed and 'mountain' bikes are very much in demand, which makes them prime targets for theft – as statistics continue to prove. Chaining the front wheel to a handy lamp-post does not prevent a determined attack on wheels or saddle either – so what can be done? Well, short of spiking the saddle with 40,000 volts or investing in a 6ft. tall Rottweiler, the humane (and legal) answer is to fit a Maplin Cycle Alarm.

Operation

Our easy-to-construct alarm kit is completely self-contained in a 129 × 64 × 44mm case, which is simply attached to one of the 'V' frame tube uprights. A special keyswitch 'arms' the system and after a short delay period the alarm will become active. Should the bicycle be tampered with, movement and vibration sensors will trigger the alarm and the sounder will give off a very loud 110dB 'screech' for 2 minutes (depending on the condition of the battery). The case can also be made tamper-proof, and a flashing red LED indicates that the alarm is in an armed state. In addition, an input is provided for connecting a push-to-make handlebar switch (not supplied) which can be used to operate the siren independent of the alarm. The PP3 type 9V battery used to power the unit should have a long operational life – provided that the bicycle is not stolen, of course!

Circuit Description

Figure 1 shows the circuit diagram for the alarm, which is based on just two ICs. S1 is a mercury switch that could be in a 'make contact' or 'break contact' state depending

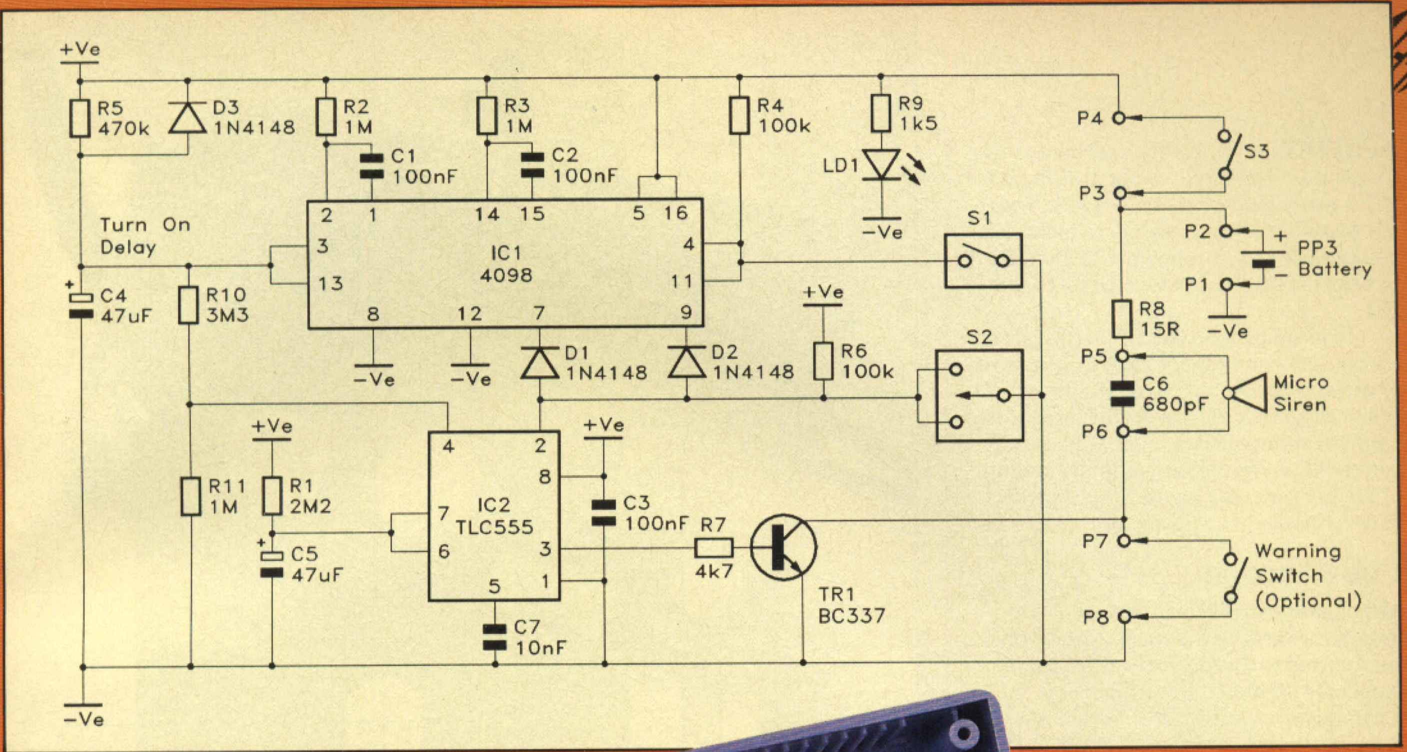
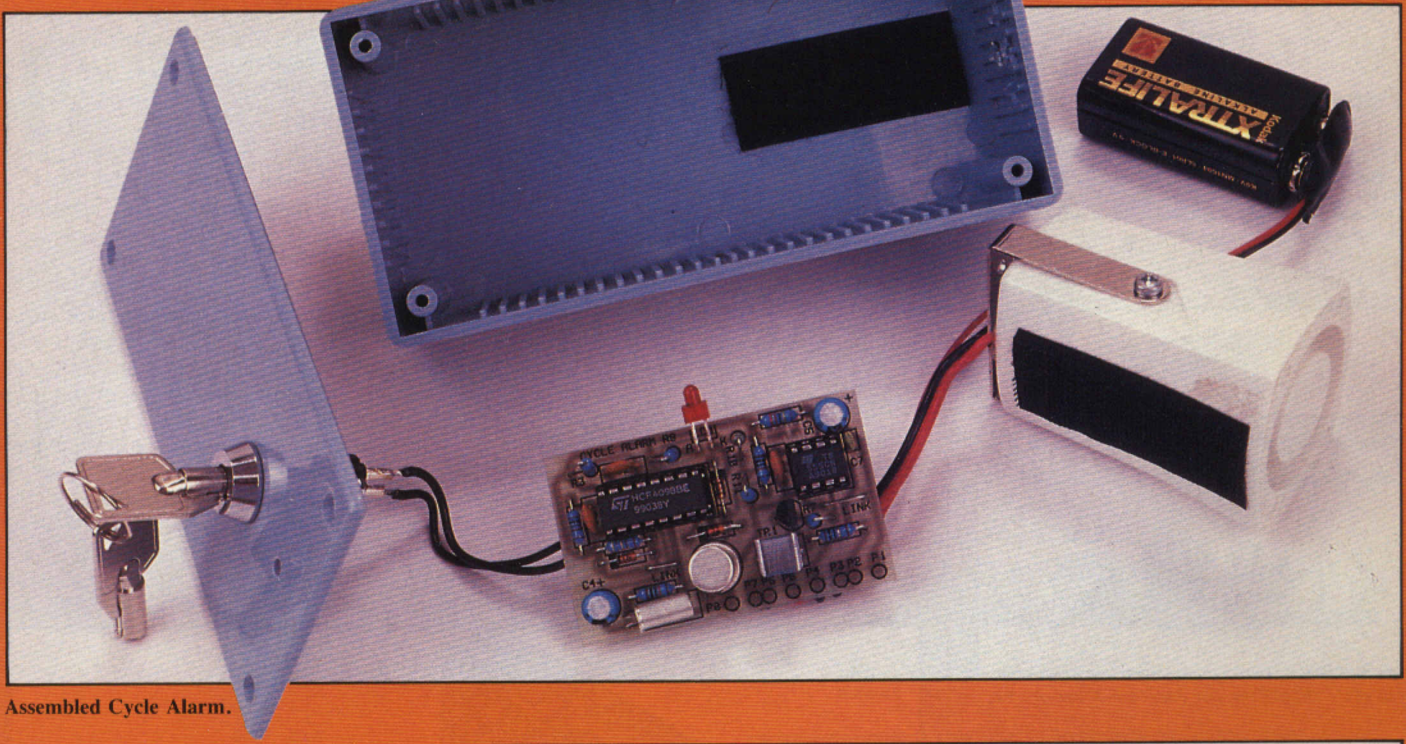


Figure 1. Circuit diagram for the Cycle Alarm.



Assembled Cycle Alarm.

upon the position of the bicycle prior to power-up. As a result, IC1 – a dual monostable – is configured for both positive and negative edge triggering by S1. The outputs of these two monostables are ORed via D1 and D2. The resulting active-low output pulse triggers IC2, a 555 timer, configured here as a long-delay monostable. The vibration switch S2 will also trigger IC2 when activated. TR1 will conduct after the 555 time-out period has expired, operating the siren. R8 has been included to limit the current consumption of the siren, ensuring a longer battery life.

As the keyswitch S3 is mounted in the case, it is possible that the vibration switch could be operated whilst arming the alarm. To prevent this possibility, a simple R/C time delay has been added to the IC1 and IC2 RESET inputs. When powering up the alarm, C4 charges slowly via R5 and holds

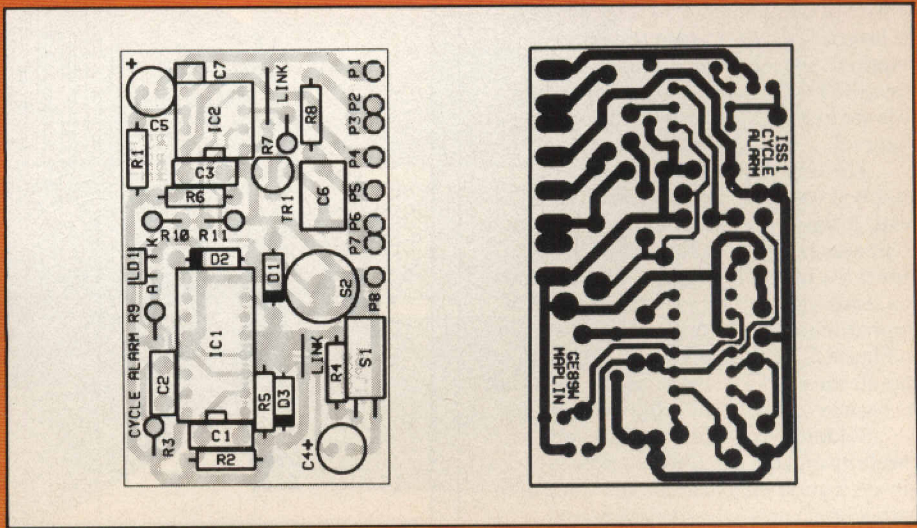


Figure 2. PCB legend and track.

the RESET inputs low for approximately 15 seconds. The reset voltage threshold for IC2 is much lower than that of IC1, and it has therefore been necessary to include a potential divider (formed by R10 and R11) to keep the reset delay time equal to that of IC1.

In its quiescent state the alarm has an average current drain of 2mA at 9V, most of which is consumed by the flashing LED. When triggered, the siren will increase this figure to approximately 80mA. Naturally, battery life is dependent upon the amount of use but generally an alkaline-type PP3 battery should have a long life.

Construction

Although construction is very straightforward, newcomers to electronics are referred to the Constructors' Guide supplied with the kit, or available separately, order code XH79L. Before fitting any components onto the PCB, two links (which can be made from spare pieces

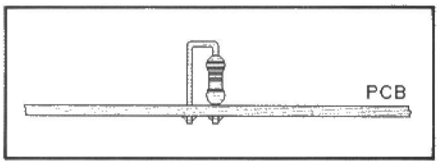


Figure 3. Mounting resistors R3, 7, 9, 10, 11.

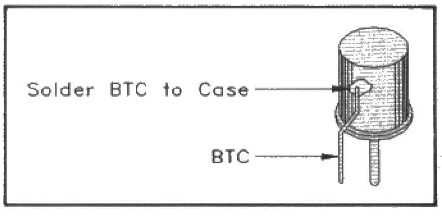


Figure 4. Preparing the vibration sensor, S2.

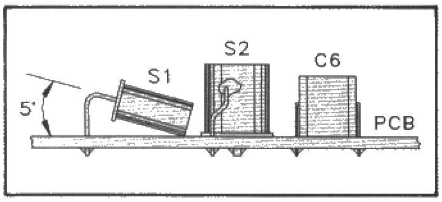
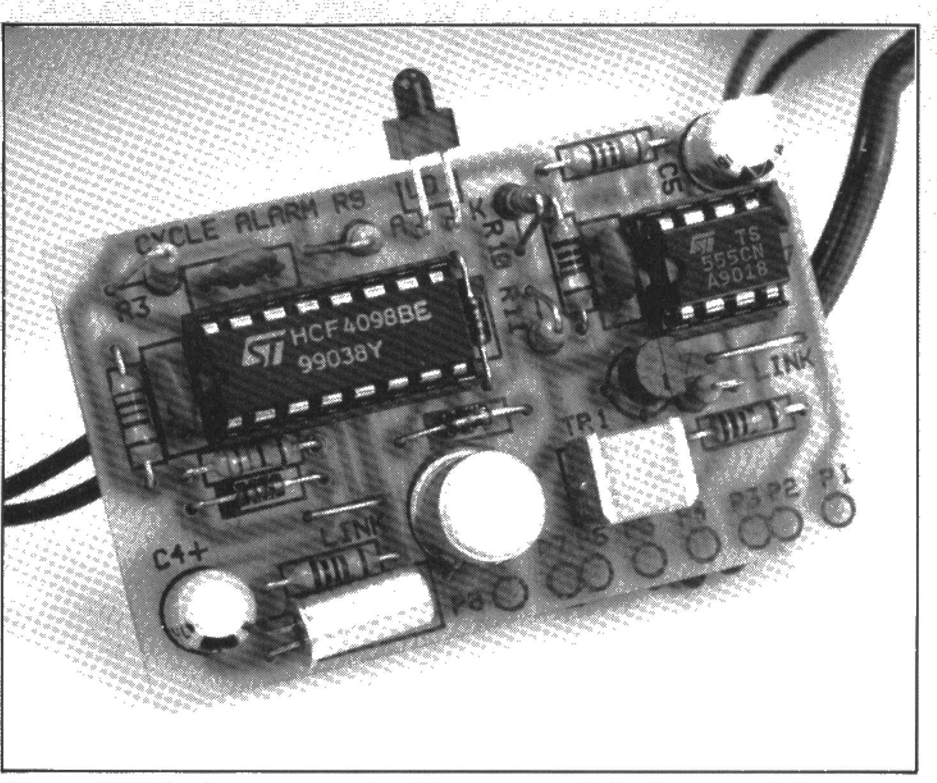


Figure 5. Installing the movement sensor, S1.

of wire or component lead offcuts) need to be inserted. Of the eleven resistors required, six are mounted horizontally onto the PCB in the usual manner while five are inserted vertically, as shown in Figure 3.

The vibration sensor, S2, may be supplied with only one central terminal lead. If this is the case, Figure 4 shows how to fit a second lead to the sensor body. Insert the movement sensor S1 and bend the leads so that the case is at an angle of approximately 5° with the PCB, as shown in Figure 5. With reference to Figure 6, mount the red LED at 90° to the PCB with its base in line with the edge of the PCB.

Solder all component leads very carefully and cut off all wire ends. It is always a good idea to scrub the track area with a brush and solvent cleaner and inspect your work at this stage!



Close-up of PCB showing correct mounting of the movement and vibration sensor switches.

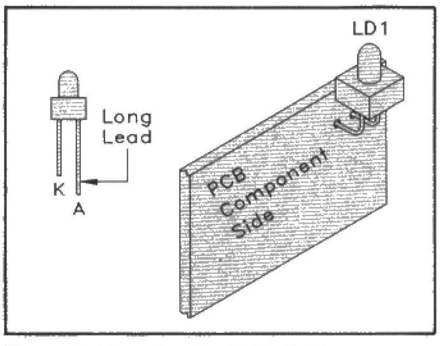


Figure 6. Mounting the LED, LD1.

Case Drilling

Although the siren sound output is loud, much of the volume would be lost if the project was to be sealed in its plastic case. A few holes are therefore required to be drilled through one end of the case – see Figure 7a. Drill a 3mm hole through the lid (for the LED) and a 12mm hole (for the keyswitch, S3) to the dimensions given in Figure 7b.

Final Assembly

The siren is fitted in the case using Velcro-mount hooks and eyes (as detailed in Figure 9) ensuring that the siren opening is positioned against, and as close as possible to, the previously drilled end of the case. Position the bracket as shown – it may be necessary to remove its securing screws to do this. The bracket will not interfere with assembly when installed in such a way, and will also provide a mounting platform for the optional 'anti-tamper' microswitch. Cut the siren supply lead lengths to 80mm and trim/tin the ends for connection to PCB pads 5 (Red) and 6 (Red/Black). Note that the wiring connections shown in Figure 10 are made directly onto the PCB track side pads and not, as is more usual, to

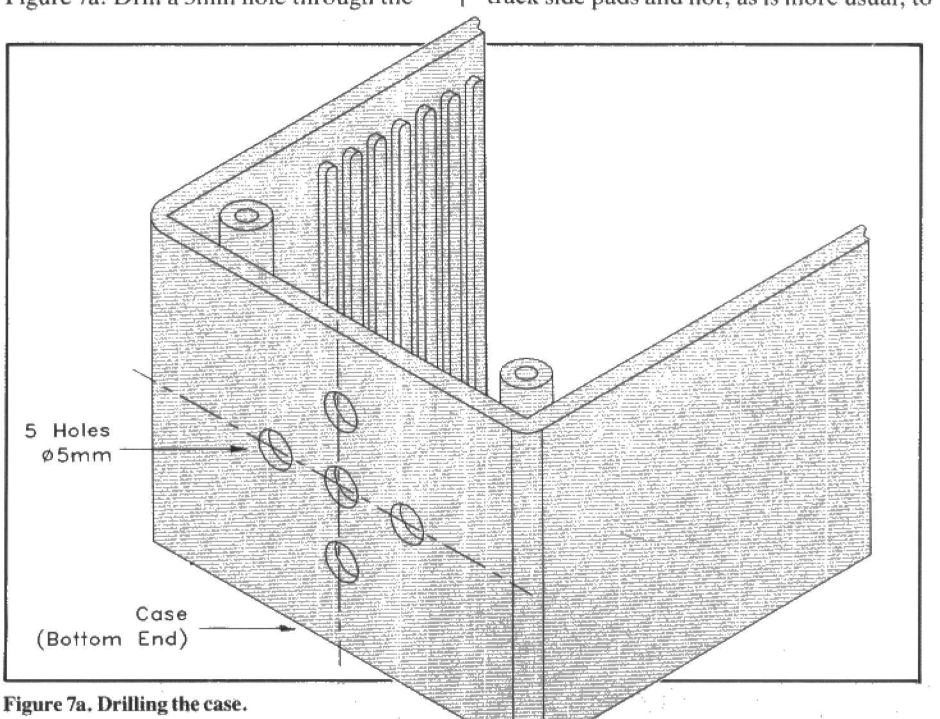


Figure 7a. Drilling the case.

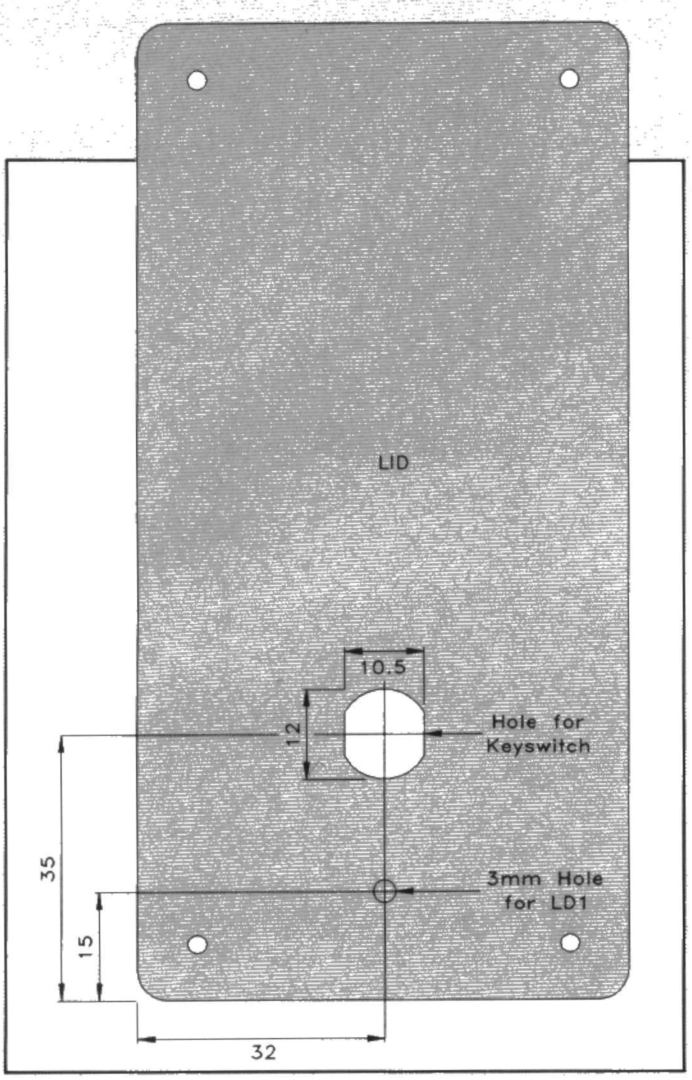


Figure 7b. Drilling the case.

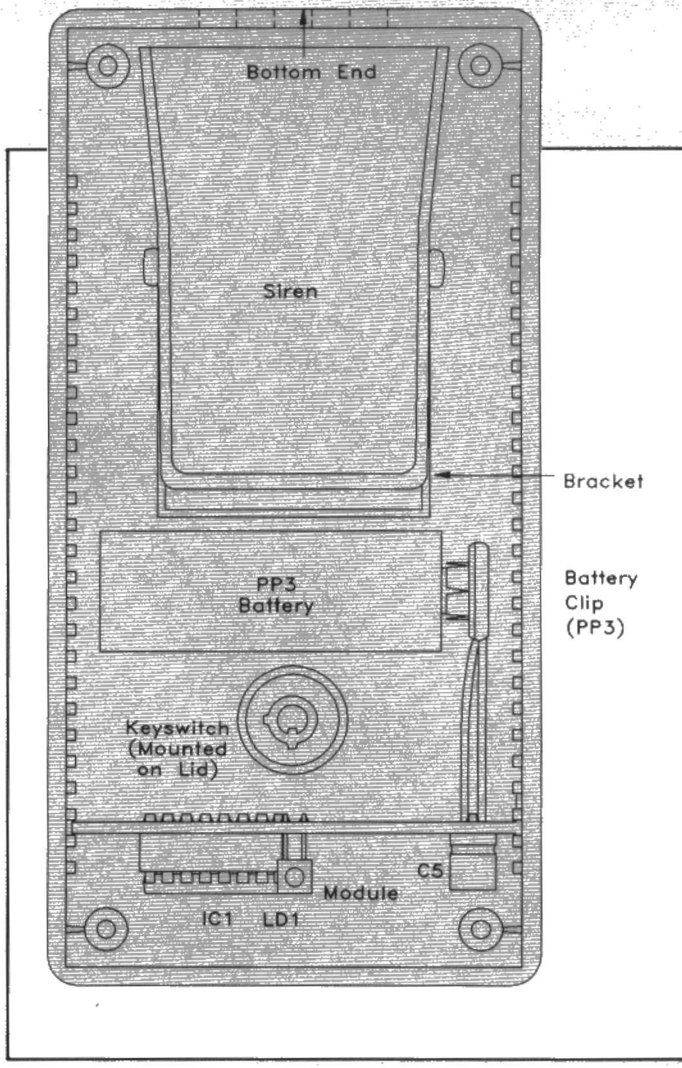


Figure 8. Final case assembly.

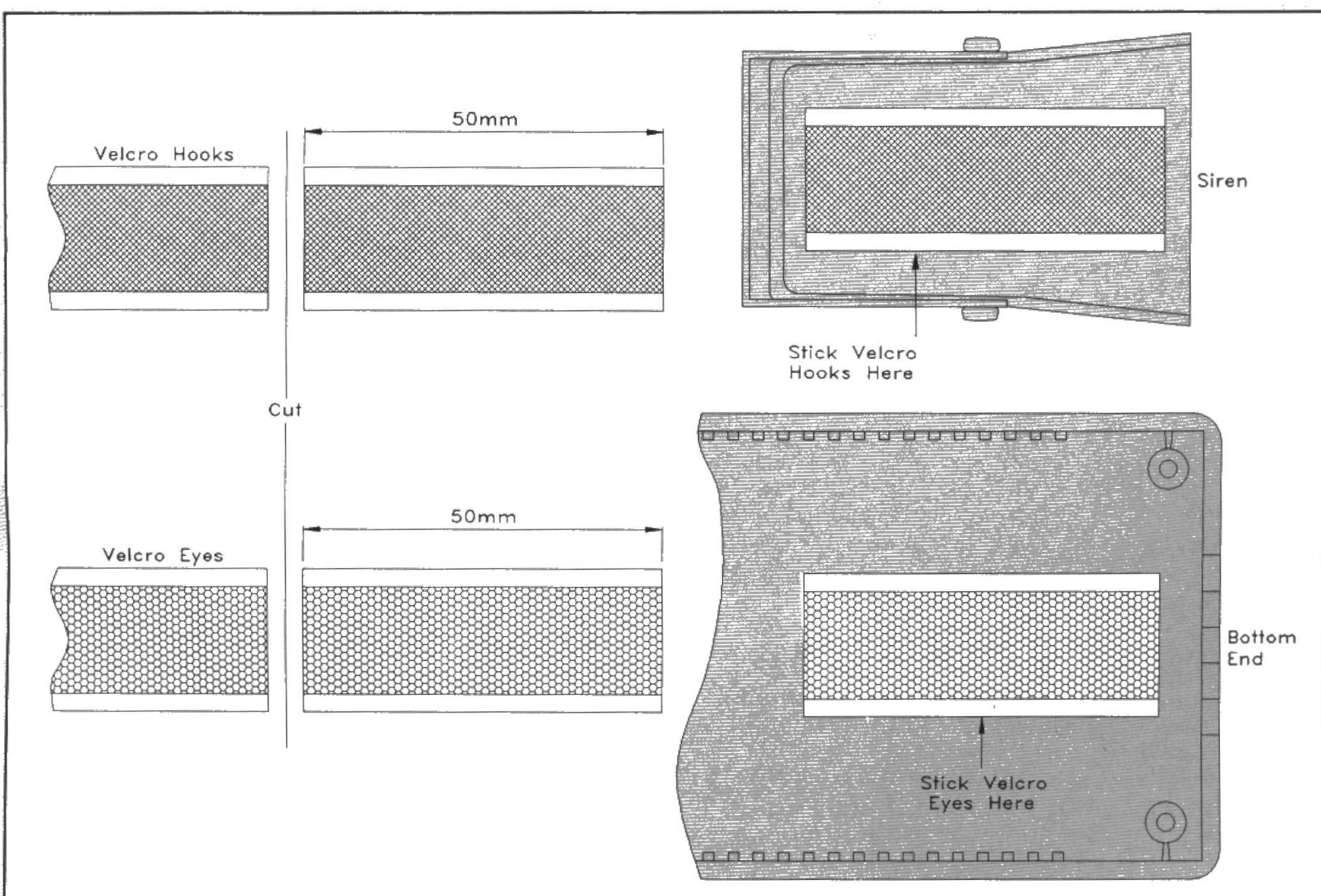
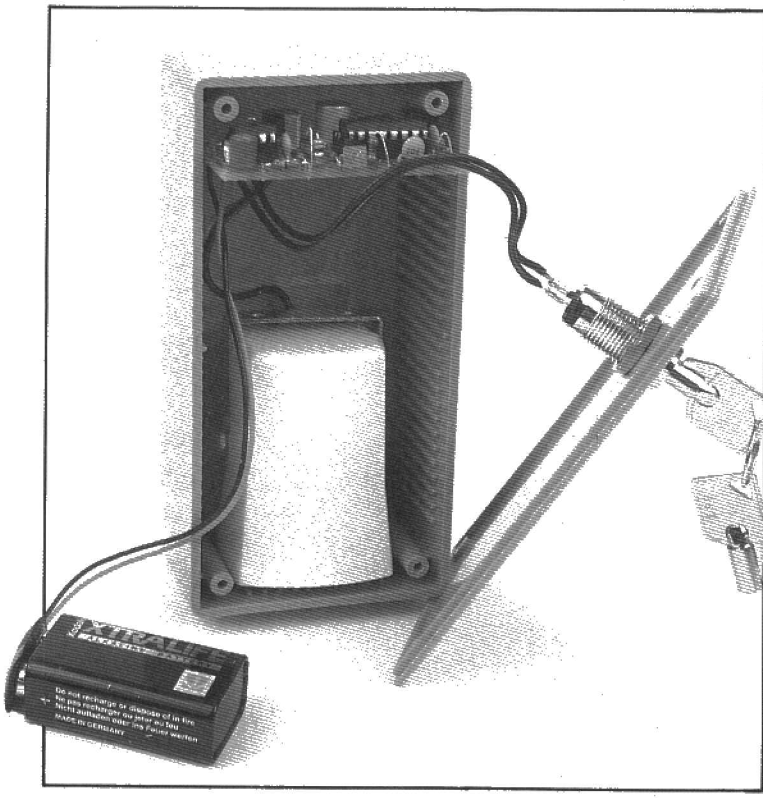


Figure 9. Mounting the siren.



The assembled Cycle Alarm with lid removed, showing internal construction.

The finished Cycle Alarm, shown fitted to a bike.

solder pins. Cut the PP3 battery clip lead lengths to 60mm and solder the Red lead (+ve) to pad 2 of the PCB, and the Black lead (−ve) to pad 1. Cut two 100mm lengths of hook-up wire and solder them to pads 3 and 4. Fit the keyswitch into the case lid hole (from the outside) and solder the other ends of both wires to its terminals. Insert the PCB into the top guide slots of the case (as shown in Figure 8), and bend the leads of LD1 so that it fits neatly into the hole previously drilled through the lid. Figure 11 shows how this is done.

If required, the optional micro-switch can be fitted for increased security. This switch is fitted to the siren (as shown in Figure 12) with the remaining pieces of Velcro, and connections are made from the Normally Closed and Common terminals of the switch to pads 7 and 8 of the PCB. If a handlebar-mounted push-to-make switch is required, it can be wired to these pads in parallel with the anti-tamper switch where fitted.

Operation

Check that the case lid fits correctly with the LED in position, and ensure that the keyswitch does not touch any of the electronics when the lid is closed. With the special key, turn the tumbler anti-clockwise to DISARM the alarm and install a PP3 battery. If an anti-tamper switch is fitted, be prepared for the siren to operate immediately!

Place the battery into the case and screw down the lid. If the anti-tamper switch (where used) has been correctly fitted, the alarm should become silent. Turn the keyswitch clockwise to begin the arming sequence and note that the LED

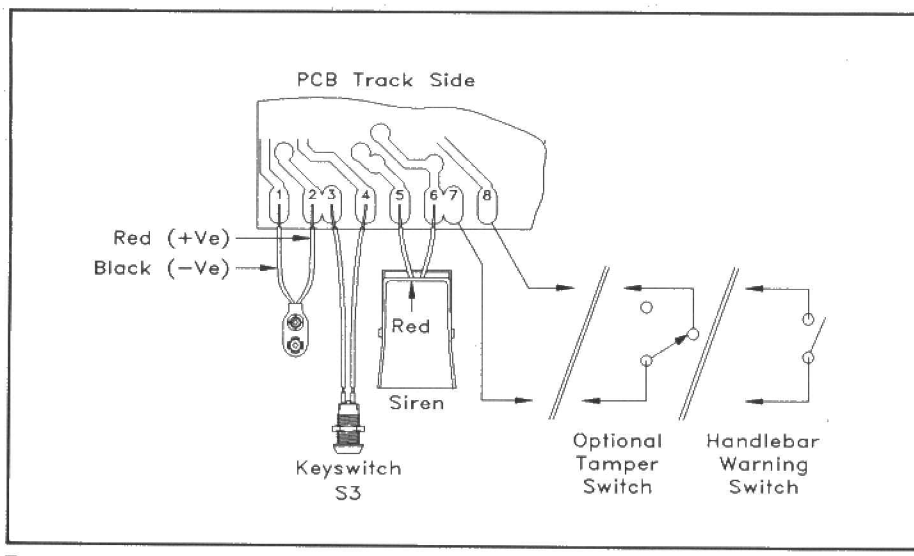


Figure 10. Wiring details.

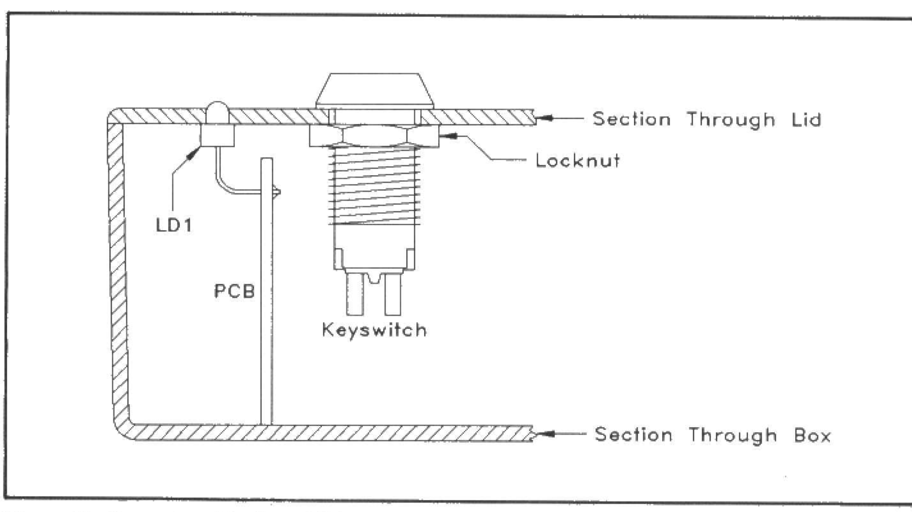


Figure 11. Correct positioning of lid components.

flashes. After several seconds have elapsed the system is automatically armed and either tapping the case or tilting it through 45° will set the alarm off. The alarm will sound continuously for two minutes or so and then reset itself, ready to be triggered again. This sequence will be repeated until the keyswitch is turned to disarm the system, or the battery runs flat.

The anti-tamper and handlebar switches will operate the siren whether the alarm is armed or not, the position of the keyswitch having no effect on these at all.

Installation and Use

The handlebar mounted switch, where fitted, allows the siren to be used as a momentary warning signal i.e. like a bicycle bell – but much louder! This feature also allows the system to be used as a personal attack alarm. Check with your local bicycle supplier for suitable switches.

Two adhesive-mounting tie-wrap bases are stuck on to the back of the case allowing the alarm to be fixed to one of the bicycle frame upright tubes with the tie-wraps supplied. The part of the frame ideal for this purpose is the seat tube. When mounting the unit, make sure that the sounder end of the case faces downwards (i.e. towards the pedals), otherwise rain and water may enter the alarm, causing corrosion.

When leaving your bicycle alarmed and unattended do not forget to remove the key. Finally, always remember to lock up your bicycle because alarms only act as a deterrent to would-be thieves and do not, in themselves, prevent theft.

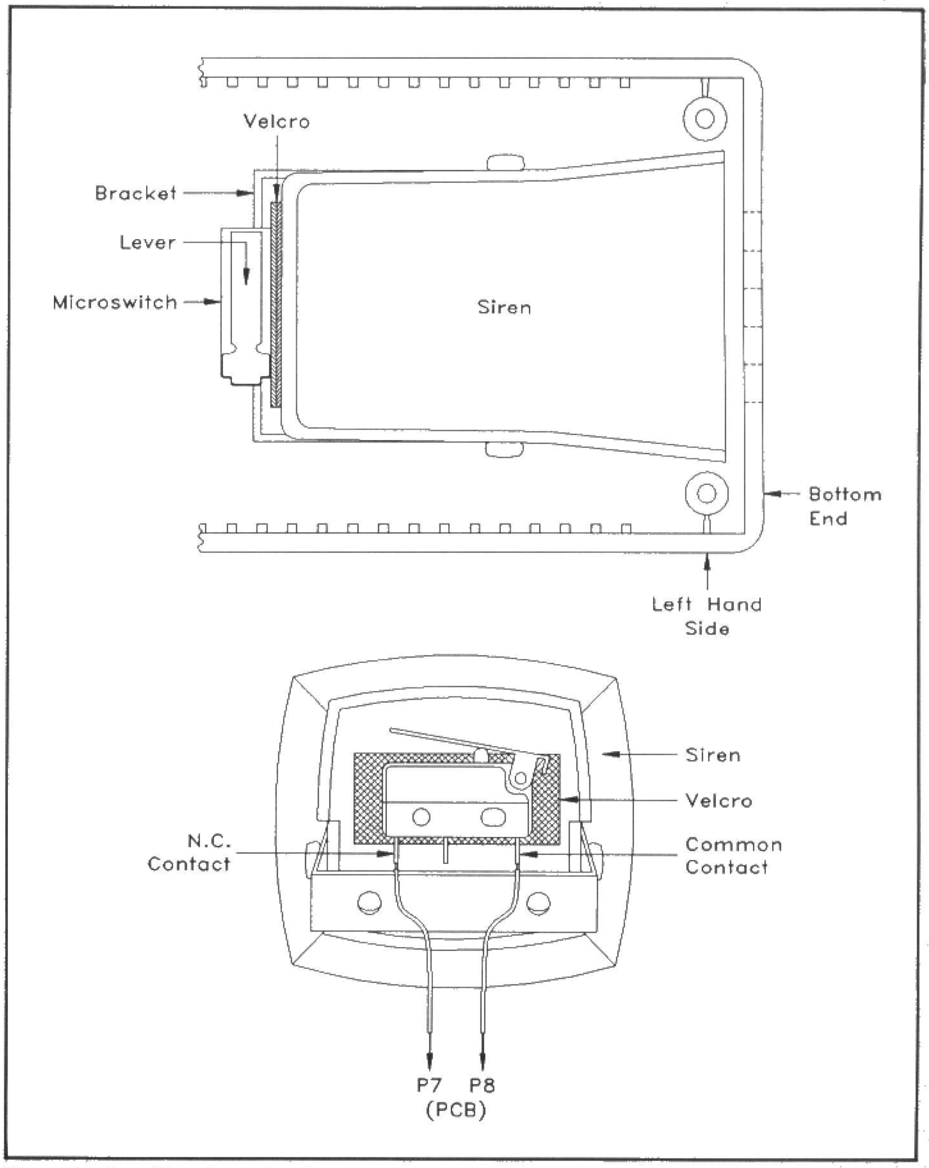


Figure 12. Installing the optional tamper switch.

CYCLE ALARM PARTS LIST

RESISTORS: All 0·6W 1% Metal Film			
R1	2M2	1	(M2M2)
R2,3,11	1M	3	(M1M)
R4,6	100k	2	(M100K)
R5	470k	1	(M470K)
R7	4k7	1	(M4K7)
R8	15Ω	1	(M15R)
R9	1k5	1	(M1K5)
R10	3M3	1	(M3M3)
CAPACITORS			
C1,2,3	100nF 16V Minidisc	3	(YR75S)
C4,5	47μF 16V Minielect	2	(YY37S)
C6	680nF Poly Layer	1	(WW51F)
C7	10nF Ceramic	1	(WX77J)
SEMICONDUCTORS			
D1,2,3	1N4148	3	(QL80B)
LD1	Flashing LED Red 3mm	1	(UK30H)
TR1	BC337	1	(QB68Y)
IC1	4098BE	1	(QX29G)
IC2	TLC555C	1	(RA76H)
MISCELLANEOUS			
S1	Min Tilt Switch	1	(FE11M)
S2	Vibration Switch	1	(UK57M)
S3	Min Key Switch	1	(FE44X)
	DIL Socket 8-pin	1	(BL17T)
	DIL Socket 16-pin	1	(BL19V)
	ABS Box PX2	1	(YU53H)
	PP3 Clip	1	(HF28F)
	Micro Piezo Siren	1	(JK42V)
	Large Cable Tie Base	2	(BF94C)
	Tie-Wrap 200/4·8	2	(FD99H)
	7/0·2 Wire 10m Yellow	1 Pack	(BL10L)
	Velcro Hooks	1m	(FE46A)
	Velcro Eyes	1m	(FE47B)
	PCB	1	(GE89W)
	Instruction Leaflet	1	(XT27E)
	Constructors' Guide	1	(XH79L)
OPTIONAL (Not in Kit)			
	Battery PP3	1	(FK62S)
	Min Lever Micro Sw	1	(FP42V)

The Maplin 'Get-You-Working' Service is available for this project, see Constructors' Guide or current Maplin Catalogue for details.

The above items (excluding Optional) are available as a kit, which offers a saving over buying the parts separately.

Order As LP76H (Cycle Alarm Kit) Price £14.95

The following new item (which is included in the kit), is also available separately, but is not shown in the 1992 Maplin Catalogue.

Cycle Alarm PCB **Order As GE89W Price £2.45**

A readers forum for your views and comments. If you want to contribute, write to: The Editor, 'Electronics – The Maplin Magazine' P.O. Box 3, Rayleigh, Essex, SS6 8LR.

Dear Editor

AIR YOUR VIEWS

Loadsa Money

Dear Sir,
I have one comment and one question to put to you following my reading of the latest issue.
The former concerns an answer you gave on the letters page to your correspondent who would like to build a CB radio. I appreciate the point you made about test equipment, but I was somewhat saddened to read you perpetuating the 'price' argument which so many magazines advance. Speaking for myself, and I hope I am not alone out here, price comes a fair way down the list when I decide whether or not to build a project, definitely below interest and knowledge with the ability to repair what I build, and a few tens of pounds more expensive would not put me off. For instance, I am not interested in CB, but have looked in vain in the magazines I take, for a design for a Hi-Fi cassette deck using some of the Dolby chips that are available. The last design that had any pretensions to quality, were the Wireless World designs in 1975 and 1976, for a deck and stand alone Dolby unit, both of which I built. Also others of your readers, like myself, may have built up a fair armoury of test equipment over the years.
On to the question, I noticed in Point Contacts column a reference to the 'Electronic Organ Constructors Society'. Could you favour me with their address?
Mr B. Fuller, Wye, Kent.

Thank you for your comments, it would certainly make life easier if we could ignore the price factor, but since we sell kits – as well as publishing the designs, the price does have to be considered. We only rule out kits if they would be grossly overpriced. Certainly, I too hope that readers regard the interest aspect of greater importance than just the price – which must of course have some bearing on the matter. On the subject of test equipment, our spectrum analyser cost £7,000! Regarding the address of the 'Electronic Organ Constructors Society', a quick telephone call to Point Contact himself obtained the required information: Mr A. T. Hawkins, 23 Blenheim Road, St. Albans, AL1 4NS. Tel: (0727) 57344.

S·T·A·R L·E·T·T·E·R

This month Mr Peter Tyler from Aughton, Lancs. receives the Star Letter Award of a £5 Maplin Gift Token for his letter on colour-blindness.

It's All in the Chromosomes

Dear Sir,
I can add somewhat to the discussion on the use of red printing, and red backgrounds, in your publications even though the problem has been resolved for the catalogue. I can comment usefully because I am one of the 1-in-30 males who are colour-blind. The corresponding figure for females is 1-in-3000 for reasons concerned with chromosomes.
By far the commonest form of colour-blindness is red deficiency meaning that red appears almost black. Thus it is intriguing to note your readers' letters in the No. 45 issue of the Maplin Magazine where the common complaint is that the red is too light. Quite the opposite for me. It was a while before I realised that the prices were red and not just a slightly lighter shade of black in the last catalogue! Not that it mattered, of course. The blue in the latest catalogue stands out much more clearly for me, if that is what you are hoping to achieve.
A much more important issue is the use of a red background in the Magazine. This appears, to colour-blind people like myself, as black on slightly lighter black, particularly in artificial light. This means that we have no chance of fast-reading such text, so we give up. It is possible to piece it together slowly if we need to, rather like guessing at the words in a crossword puzzle when you have managed to fill in a few of the letters. Examples in the No. 45 issue are pages 8/9, but pages 32/33 are hard work also.
So I am afraid this particular publishing gimmick (used in other publications also) has an entirely negative effect for 3% of your readers. Any background colour except red I would say.

Thank you for your comments, we now have a better idea of the problems that colour-blind people encounter with the magazine. It would be interesting to learn if other colour combinations result in similar problems – apart from personal taste for colour that is!

Get You Working?

Dear Editor,
Just a small point, why is the MIDI Switch Box covered by the 'Get You Working' Service, where the only problems could be a wrong PCB or faulty sockets/switch, while other, far more complicated units aren't, e.g. MSM6322 Pitch Controller or L200 Voltage/Current Regulator? You are trying to have your cake and eat it – offering a very attractive service, but not to those who can't solder a switch and a few sockets onto a ready made PCB.
J. Ogden, Hemel Hempstead, Herts.
P.S. I may not be a beginner, but I certainly need some help!

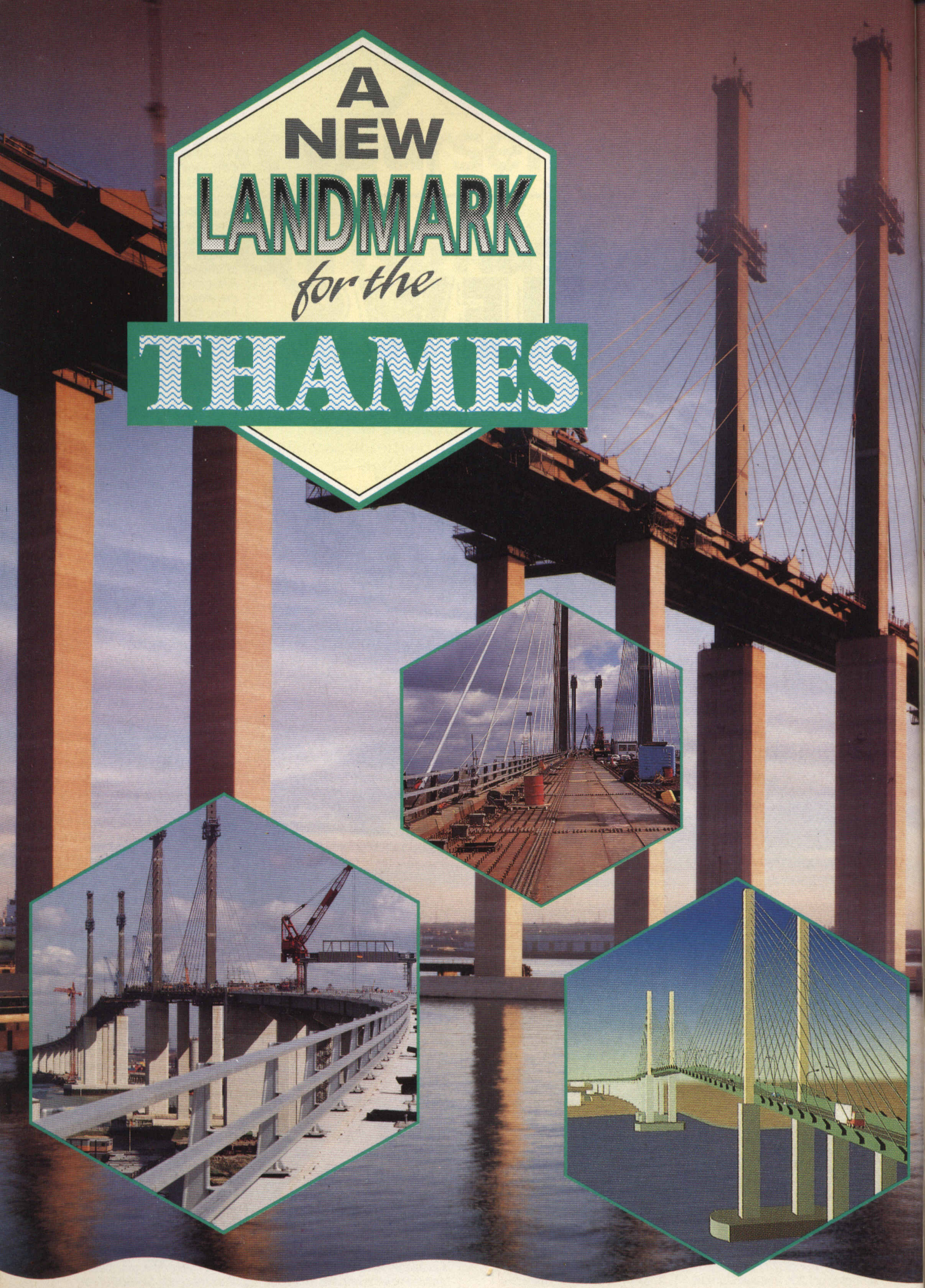
Thank you for raising the point, I am sure that many other people have wondered the same thing. The answer is really quite simple, the 'Get You Working' Service is available for all fully fledged projects. Still confused? To quote the 'blurb' from page 79 of this issue, which gives information about the Service:
"The 'Get You Working' Service is available for all Maplin Kits and Maplin Projects with the exception of 'Data Files'; projects not built on our ready etched PCBs; projects not built with the majority of components supplied by Maplin; Circuit Maker ideas; Mini Circuits or other similar 'building block' and 'application' type circuits"
Since the MIDI Switch Box is a fully fledged project, it is automatically covered by the Service. The MSM6322/L200 projects are 'Data File' type projects and are therefore not covered. The reason being that 'Data Files' are experimenters circuits, i.e. designed to have the component values modified and therefore perform differently to the original published design. Hopefully you can now see the problem – how can the repair engineer be (reasonably) expected to get working a circuit, when the circuit may have been modified to perform a drastically different function? The same reasoning applies to other 'building block' type circuits.
Taking the MIDI Switch Box and the 'Data Files' in isolation doesn't present a true picture – it is worth remembering that projects such as the multi-board NICAM TV Tuner unit are covered by the Service. However, for technical queries, help is available on all Maplin projects and products (including 'Data Files'!); see page 79 for details.

Timely Advice

Dear Sir,
Last year, when I came to that annual problem of non-working Christmas tree lights, I removed all the bulbs and tested them on my bench power supply. As all the bulbs worked, I was confident that when refitted, the lights would work, but no luck!
At this point, I was thinking either of giving up electronics or buying some new lights, or both – when inspiration struck. First I checked that the return wire which ran the length of lights was connected to the neutral pin of the plug, then I stretched the lights out over the sofa and ran my Maplin Live Wire Detector along the string of lights and located the fault instantly. This turned out to be a bulb with an unusually small blob of solder, soon rectified with an instant iron.
The moral of this is, use your Maplin Live Wire Detector first!
Jan Chapman, Bradford, West Yorkshire.

Thank you for the advice, since this issue is on sale from the 6th December, it may be just in time to help some other frustrated readers! Incidentally, last issue's special offer of a 10% saving when buying the Live Wire and Mini Metal Detectors together, is available until 31st December 1991. Remember you must use the order code MMS00 or you won't benefit from the saving!

A NEW LANDMARK for the THAMES



The latest addition to the South-Eastern English landscape has a major new technological tale to tell. The Thurrock-Dartford bridge, which opened in October 1991, will be the third means of crossing the lower Thames from Thurrock, Essex into Dartford, Kent. It features four southbound-only lanes, along with margins and emergency footways. Eventually, both tunnels will be used for all north-bound traffic, and the bridge will be used to carry all vehicles travelling south to Kent. If exceptionally high winds are noted (remember late 1987 and early 1990?), the bridge will be closed to traffic and the Tunnel will temporarily revert back to its original system (2 lanes northbound; 2 lanes southbound). It is clear to see that the introduction of the Bridge represents a doubling of the original (tunnel) capacity. This will be of great advantage when the Chunnel finally opens, and travellers and freight make their way to Kent en route to France (no pun intended!) and the rest of Europe.

The Thurrock-Dartford bridge is the first crossing in Britain to be equipped with Automatic Vehicle Identification, or A.V.I. This is a means of sparing motorists the bottleneck-creating and time-consuming toll-booth rigmarole which might otherwise be expected whenever the Bridge is used. Drivers who use the Dartford Tunnel will understand exactly what is meant here! So, while the Bridge itself represents a major engineering and transport milestone, electronically A.V.I. is quite unique too.

Congestion

The need for a third river crossing in this area dates back to the opening of the second Dartford Tunnel in 1980. This Tunnel doubled capacity from 30,000 to 60,000 vehicles a day. These levels were sustained and then took an enormous leap in 1986/7 when the Tunnels formed the eastern link of the M25 (Europe's Largest Roundabout?) Traffic now averages 70,000 vehicles daily, with occasional peaks of 90 (or even 100,000) vehicles a day contributing to the notorious congestion at this point. Even in these difficult times, traffic is destined to grow at 3% per year into the next century.

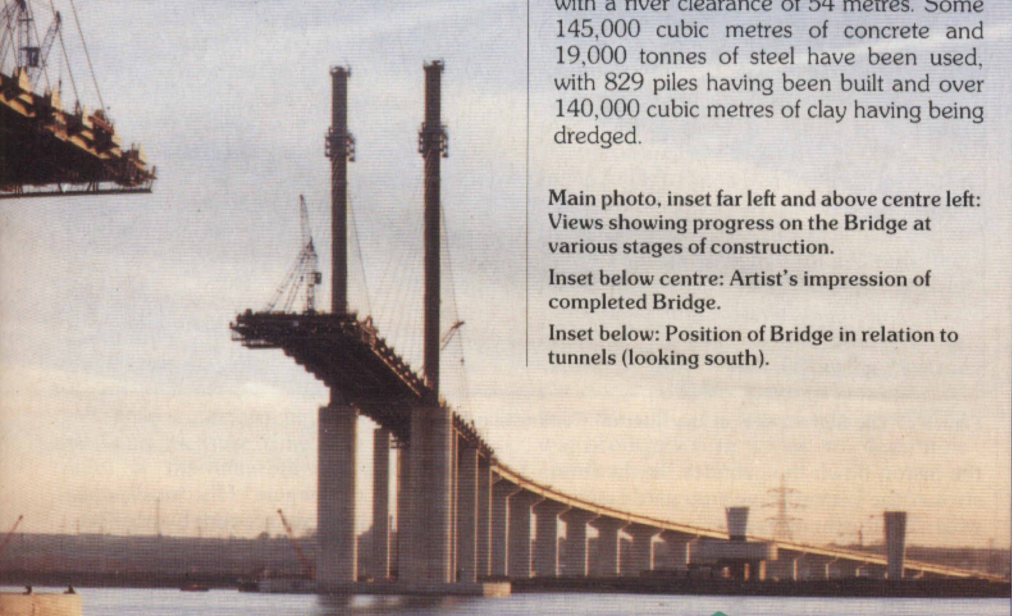
The Government therefore sought a means of improving traffic flow, while providing the much needed extra capacity. They invited private sector bids for the crossing, and in 1986 awarded the contract to Dartford River Crossing Limited – a consortium of Trafalgar House, Kleinwort Benson, Prudential Assurance and the Bank of America.

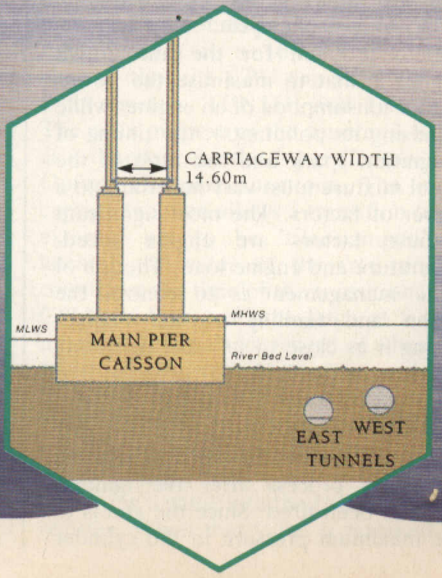
The bridge is a cable-stayed structure with approach viaducts, construction of which commenced in July 1988. It has a main span of 450 metres (supported by a pair of steel towers on top of reinforced concrete piers), with 180 metre long back spans on each side of it. The total length of the Bridge itself is 812 metres while the overall crossing is 2870·7 metres in length. The main pier towers are 137 metres high with a river clearance of 54 metres. Some 145,000 cubic metres of concrete and 19,000 tonnes of steel have been used, with 829 piles having been built and over 140,000 cubic metres of clay having being dredged.

Main photo, inset far left and above centre left: Views showing progress on the Bridge at various stages of construction.

Inset below centre: Artist's impression of completed Bridge.

Inset below: Position of Bridge in relation to tunnels (looking south).





Toll Collection

By any measure the Bridge is a major project. The arrangements for establishing and running it are also a first for Britain. The Bridge has been built using entirely private sector money. The company, formed by Trafalgar House and its partners, first had to pay £43·5m for the existing Tunnels, which they now operate. They have signed an agreement to operate both Tunnels and the Bridge for a maximum of 20 years. Tolls will be linked to inflation and the company can only charge Government-agreed tolls linked solely to the Retail Price Index. In no more than 20 years, the organisation must hand the bridge back, unencumbered, to the Nation.

Upon current projections the Company will have repaid the £86m capital cost of the bridge within 14 years. By that time the company will have made profit through the building and maintenance of the bridge, but more importantly they will have established themselves in an important new area. They will also have gained valid experience which will be of great benefit when becoming involved in any future private road schemes.

Such a radical social and engineering change also demanded some innovative electronic thinking. The existing toll-collection arrangements were recognised as being unable to cope with the advent of a further doubling of capacity brought about by the Bridge coming into operation. The layout of the roads and the limitations of the surrounding area meant that the current staggered 12-lane plazas on each side could not be extended. These arrangements are conventional with a mix of manual and automatic collection systems. The manual system works through a processor-based audit control system, accepting all types of vehicles. Each manual system features an axle counter to check on the accuracy of the Operator. The Automatic system is restricted to cars and incorporates a fast-acting barrier.

As a result of this potential overload the company commissioned, in 1989, a study into methods of increasing toll collection capacity. They also wanted to further reduce costs, reduce the amount of cash carried to stop fraud, and also ensure good traffic flows.

A.V.I.

For these 1989 trials two systems were evaluated: one manufactured by European electronics giant Philips; and the other supplied by Amtech, based in the USA. These systems were installed in existing operational automatic toll lanes, using the detector loops of the present system. Thus, their performances could be compared and evaluated.

System Tests

During the month of June 1989, a number of regular prepaid ticket holders were invited to take part, answering questionnaires about their use of the system.

The PREMID system from Philips

Continued on page 30.

MICROCONTROLLERS IN AUTOMOTIVE APPLICATIONS

PART TWO by Jeff Wright BSc (Hons)

Introduction

In part one of this series, the concept of using microcontrollers in automotive applications was introduced, along with descriptions of electric window and central locking systems which use such devices. In this issue, we will look at other systems which rely upon, or are greatly improved by, microcontrollers.

Engine Management

Engine management in this context means having complete control over an engine's ignition timing and fuel mixture on a cycle-by-cycle basis. The trend in increasing engine management performance has been driven by the tightening of emissions regulations around the world. This is the real performance end of the microcontroller market and it has been responsible for the growth in complexity of the μC's on-chip timer systems, for as we will see, engine management involves a lot of time-critical tasks. Before discussing where microcontrollers fit into this application, a brief explanation of what is involved in engine management and how it has been tackled in the past would be beneficial.

Figure 1 shows the four stages of a complete cycle of a four-stroke internal combustion engine. In the first stroke, the piston is travelling downwards with the inlet valve open, thus drawing in the air/fuel mixture from the inlet manifold. In the second stroke, the piston rises with both valves closed, thereby compressing the mixture. As the piston reaches the top of its travel (Top Dead Centre or TDC), the spark plug is fired to ignite the mixture. The third stroke is the combustion/power stroke, when the cylinder delivers its power; the rapidly combusting mixture becomes very hot and the resulting rapid increase in pressure drives the piston down the cylinder. In the final stroke, the piston travels upwards again, with the exhaust valve open, thus expelling the remaining burnt gases. The piston is then ready to start its next downward intake stroke, and so initiate another four stroke cycle.

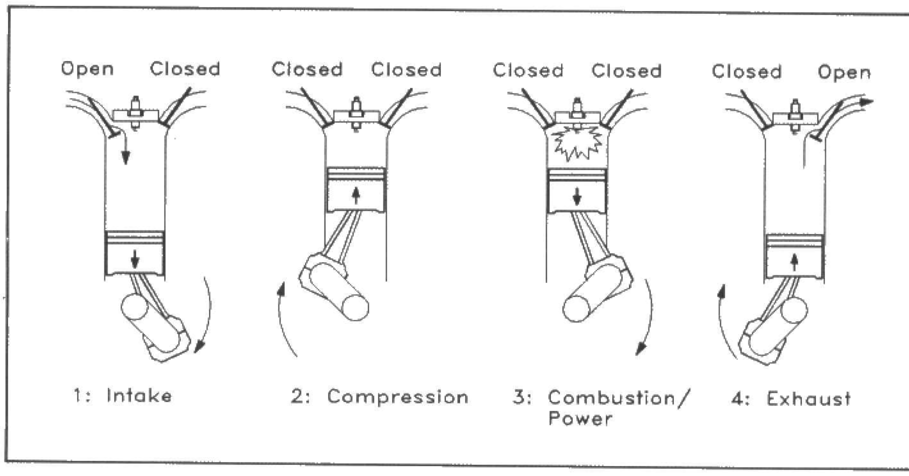


Figure 1. The four strokes of the Internal Combustion Engine.

The problem for the automotive designer is that to maximise the power and fuel consumption of an engine (while minimising its pollutants), the timing of the ignition spark and the ratio of the air/fuel mixture must vary according to a number of factors. The most significant of these factors are engine speed, temperature and engine load. The job of engine management is to control the ignition and fuelling of the engine, keeping it as close to its ideal operating conditions as possible.

Ignition

On average it takes 2ms to complete the combustion process after the ignition spark has been fired. Since the aim is to have maximum pressure in the cylinder just after the piston has passed the top of its stroke (too early and the pressure would inhibit the pistons upward travel; too late and power is wasted in the downward stroke), it is necessary to fire the spark before the piston reaches TDC. It is customary to represent this 'ignition point' as the number of engine degrees before top dead centre (BTDC). As the piston travels faster and faster with increasing engine speed, and because the combustion process takes the same length of time, a fixed firing angle for the spark would result in maximum pressure occurring further and further into the downward stroke, so wasting power and increasing fuel consumption. For this reason the ignition point must be advanced (more degrees BTDC) with increasing engine speed. Traditionally this has been accomplished with the centrifugal advance mechanism in the distributor. Another factor which influences the ignition timing is the engine load, which can be shown to be proportional to the amount of air inducted by the engine. Historically this factor was taken into account by connecting a pipe from the inlet manifold to the distributor advance mechanism (the vacuum advance). This mechanical system (which has remained virtually unchanged for many years) is reliable, but only allows crude control of the ignition timing, resulting in compromises in the engine performance and great difficulty in reaching today's emission regulations.

Mixture Control

For an engine to run well, a specific air/fuel ratio must be maintained. The theoretical ratio of fuel to air for complete combustion (and therefore maximum economy and lowest emissions) is just under 1:15 in weight (or alternatively 1L of fuel for every 10000L of air in volume). In practice, maximum fuel economy is obtained with around 20% excess air, while maximum power is obtained with approximately 10% air shortage. Since engines normally run at

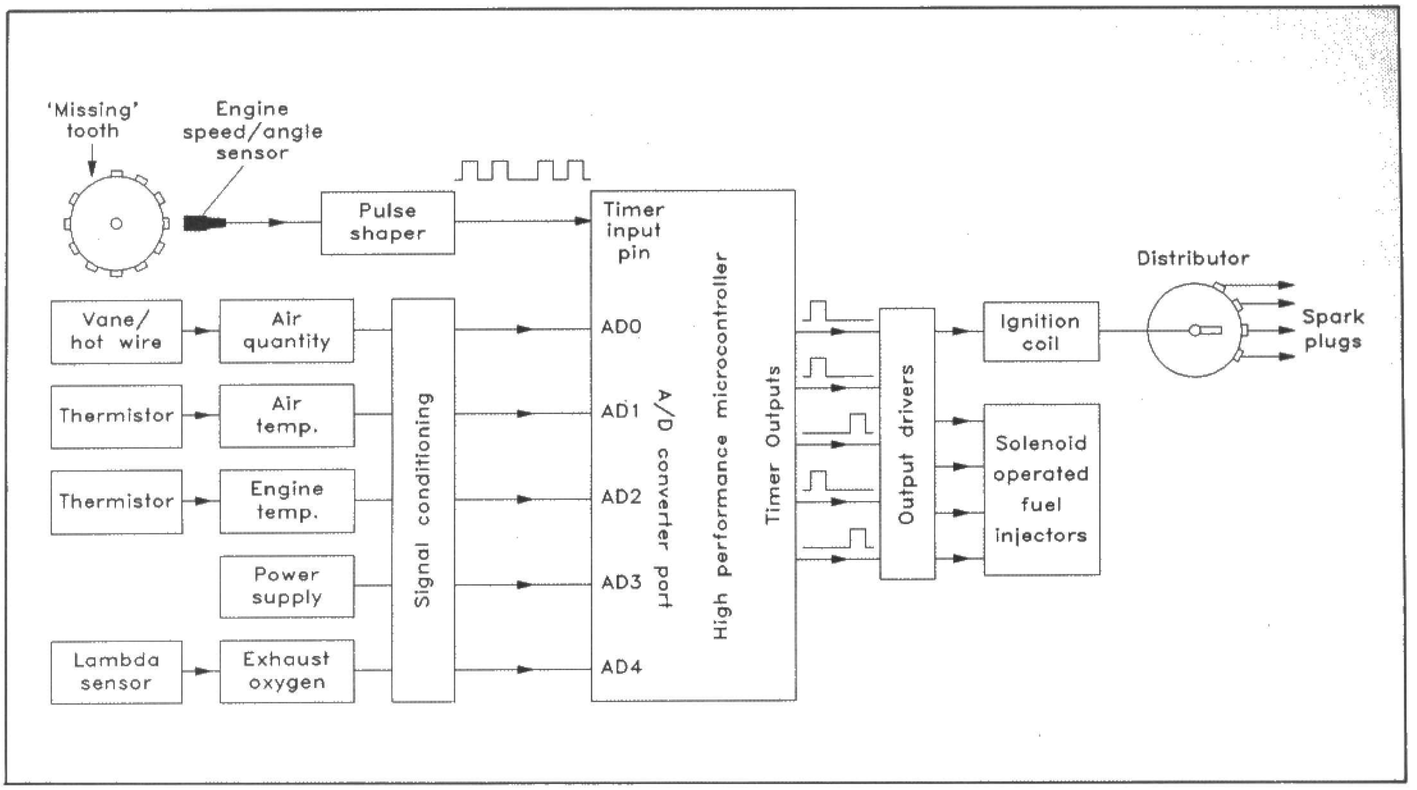


Figure 2. Simplified block diagram of an Engine Management System.

part-load, the fuel system is designed for maximum economy at this point and the mixture will be richer at idle and maximum power. The task of the carburettor, or fuel injection system, is to produce the best mixture for the engine under its current operating conditions. The simple mechanical carburettor again compromises the fuel mixture under different conditions and the trend today is towards electronic fuel injection, where a precise amount of fuel can be delivered to the individual cylinders.

Since ignition timing and fuel mixture are both dependent on the same variables (engine speed, load and temperature), it makes a lot of sense to combine the control of both into a single unit – the so-called electronic engine management system. With its ability to read sensors, perform high-speed calculations and measure time, the microcontroller is the ideal device for engine management.

Figure 2 shows a block diagram of a typical system based on a high-performance microcontroller. Engine speed and angle are both obtained from a single inductive sensor that generates electrical pulses when teeth on the flywheel pass by. To provide a reference point for determining the engine angle, either one or more teeth are omitted from the flywheel, thus producing a pulse period twice or more than the normal. Alternatively, but less common, an extra tooth may be present resulting in two pulses each of half the normal period. This means that to determine engine speed and angular position, the microcontroller must perform two basic tasks:

i) It must detect the missing/extra tooth and then count teeth to determine the engine angle.

ii) It must track the time between adjacent teeth, and from this calculate the current engine speed.

Since there are typically 30 to 60 teeth on the engine flywheel and a typical engine has to be designed for an 8000rpm maximum, the pulse period from the flywheel sensor can be less than 125μS. Clearly then, if the μC used software loops to count the periods of the incoming pulses, there would be very little processing time left to use the data obtained, even if it didn't have other signals to measure as well. For this reason independent timer systems on board the microcontroller have evolved to lessen the load on the CPU. These timers use an 'input capture' mechanism to 'time tag' incoming pulse edges against a free running counter timebase, and then interrupt the CPU to tell it to read the captured time. The following section illustrates how the timer system interacts with the CPU on Motorola's M68HC11 microcontroller in order to determine engine speed and angle:

The diagram in Figure 3 shows a simplified block diagram of the Timer and Pulse Accumulator systems onboard the Motorola M68HC11 MCU, a particularly popular device for current engine management solutions. The heart of the timer system is a 16-bit free-running counter that the CPU can read via two 8-bit registers, TCNTHI and TCNTLO. The main purpose of the counter is to act as a timebase for the Input Capture and Output Compare functions. The input capture function allows a transition on an external pin to be 'timestamped' by latching the value of the free-running counter at the time of the transition. The CPU can then read the latch at a later time and get an exact record of when the transition occurred. The output compare, or match, function is the inverse of the input capture; it allows the CPU to schedule a change in the state of an output pin, at a precise time in the future, by writing a value into the 16-bit compare register. When that value is matched by the incrementing free-running counter, the output will change state. The M68HC11 has various combinations of input capture and output compare pins available on several of its family members. The pulse accumulator is an 8-bit counter that is clocked by a specified transition on an external input pin. The CPU can write any value into the counter, and can read it at any time. The pulse accumulator can generate an interrupt to the CPU when it overflows.

The timer module and pulse accumulator can be used in a number of ways to determine engine speed and angle, and to generate the necessary output pulses. The following is one such method:

The conditioned signal from the flywheel sensor is connected to both the pulse accumulator input pin and input capture pin. Both the input capture pin and the pulse accumulator pin are configured to detect a rising edge, and the input capture interrupt is enabled so that the CPU will be interrupted on every pulse rising edge. The interrupt software routine will read the captured value of the free-running timer, store it and then subtract the last captured value, to obtain the tooth pulse period in timer counts. Since the number of teeth are known, the engine speed can easily be derived from the pulse period. Since the period of every pulse is measured, the interrupt software can identify the longer period associated with the missing tooth angular reference. At this point it can clear the pulse accumulator, which will then start counting pulses (teeth). Since each tooth corresponds to a number of engine degrees, the value of the pulse accumulator is a representation of the engine angle. To generate one of the output pulses (e.g. for an injector), the input capture interrupt software can check the pulse accumulator against the desired tooth count (minus 1 or 2, to allow for interrupt latencies). When the pulse

accumulator matches this value, the CPU can schedule the start edge of the pulse by reading the free-running counter, adding an offset and writing the resultant value into the output compare register of the desired pin. The offset is a value in timer counts that corresponds to a number of engine degrees at the current speed. This number of engine degrees is the difference between the angle matched to the pulse accumulator value and the exact number of engine degrees at which the pulse must begin – see Figure 4.

The other input parameters of Figure 2 are measured using an analogue/digital (A/D) converter, which is usually integrated on-chip as part of the microcontroller. As previously mentioned, the air inducted by the engine can be used as a measure of the engine load. A value for this is obtained, via a vane device in the air intake that operates a potentiometer, or alternatively via a hot-wire sensor. The lambda sensor is a fairly recent addition to engine management systems prompted by increasing anti-pollution regulations that have led to the use of catalytic converters. The catalytic converter is a delicate object and very stringent control of the engine emissions must be obtained if the catalytic converter is to operate efficiently. The lambda sensor is basically a hot platinum/ceramic device that produces an output voltage which varies, depending on the oxygen content of the gas it is surrounded by. By inserting such a sensor into the exhaust manifold, it is possible to determine the air/fuel composition currently being burned in an engine. This effectively transforms the engine management system, from an open-loop control system into a closed-loop one, where deficiencies in the desired output (correct air/fuel mixture) can be detected and the input variables (ignition timing/fuel quantity) adjusted to compensate. This means that much closer control of the exhaust emissions can be maintained, helping to maximise the efficiency of the catalytic converter mounted downstream in the exhaust system.

Having measured all these parameters, the microcontroller must determine the corresponding outputs – i.e. the timing of the spark ignition pulses, and the timing/duration of the pulses which fire the fuel injectors. This is achieved by accessing the so-called 'engine maps' that are stored in the memory of the microcontroller. These maps are, in fact, tables of data that hold the ignition and fuelling characteristics of a particular engine type against a number of input variables. Since it is impractical to try and store all the possible combinations of output timing vs. input characteristics, a number of points are held in the map table, and the µC must then perform an arithmetic calculation to interpolate between the two closest points given, to the exact input conditions obtained from the various sensors. Since there are a number of variables to be taken into consideration, these interpolation calculations are complex and require a lot of processing power to be completed quickly, in time to set up the output timings for the next engine cycle. This is the reason why 16 and now 32-bit microcontrollers are replacing the older 8-bit systems for engine management. They allow more complex calculations to be completed quickly so that closer control can be maintained on a cycle-by-cycle basis. When the microcontroller has obtained the desired output timings, it must

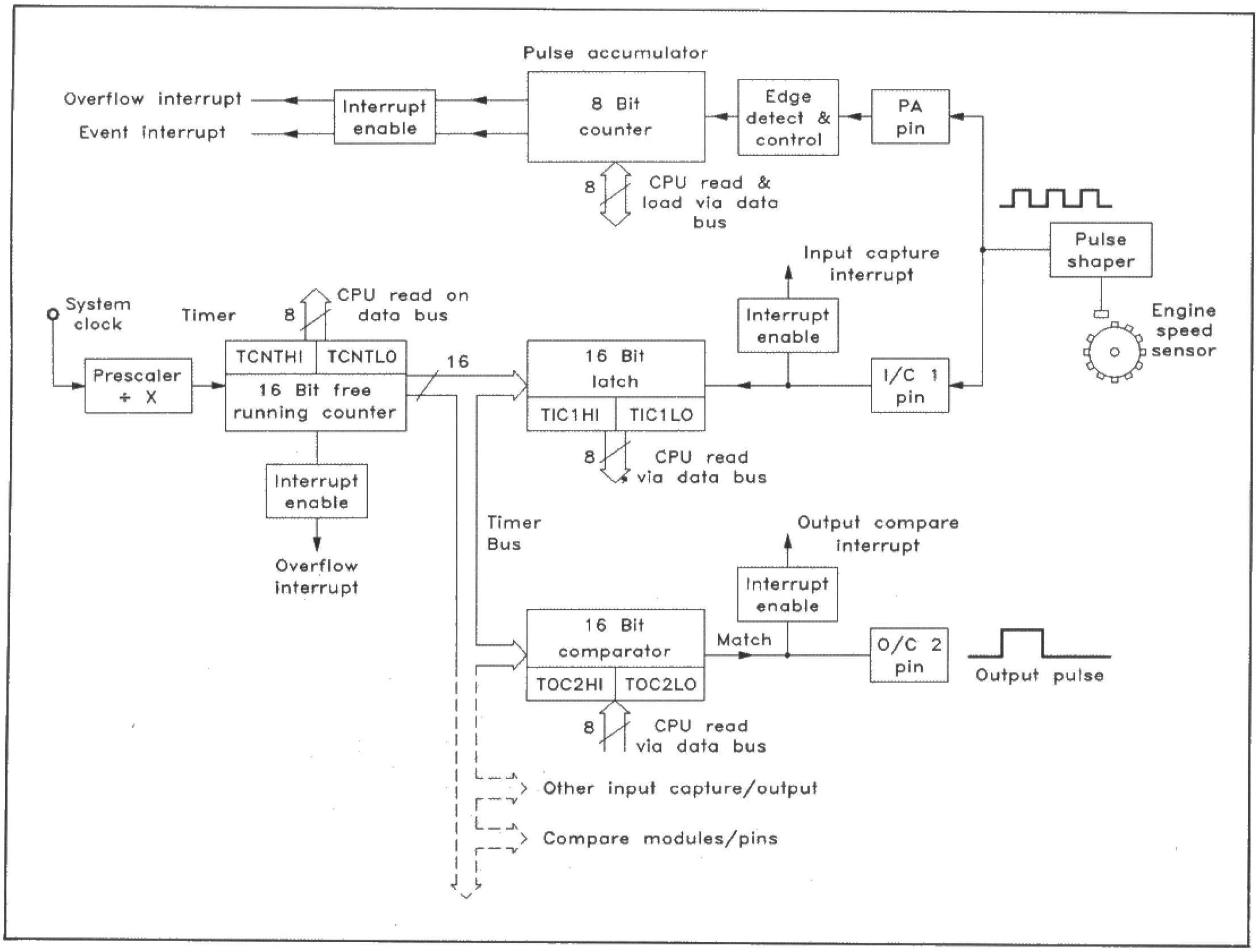


Figure 3. Simplified functional block diagram of the MC68HC11 Time/Pulse Accumulator System.

actually generate the pulses to fire the spark plugs and injectors. This is done via the 'output match' facility of the timer system, where the CPU writes a value into a special register. When the value of the incrementing timer-counter reaches the same value as that in the register, the hardware of the timer system automatically changes the output pin state to a desired level. This mechanism allows very accurate placement of the various pulses required in the engine cycle, as we have seen from the description of the Motorola M68HC11.

The method described above using the input capture and output match timer functions is used in virtually all of today's production engine management systems. However, this system is still not perfect as the CPU still has to respond to a large number of interrupts generated by the timer, thus slowing down its control calculations. This 'interrupt overhead' has set the performance limits of today's systems, and so a new approach will be required for the even more complex control algorithms required for tomorrow's emission regulations. Motorola has been the first microcontroller manufacturer to address this problem by introducing the innovative MC68332 device. Not only does this device have a powerful 32-bit 68000-based CPU, but is unlike any other microcontroller in that it also has a second on-board CPU dedicated to controlling timer functions. This Time Processing Unit, or TPU, is in effect a microcontroller within a microcontroller! The TPU is used to handle almost all of the interrupts associated with the timer channels, thus freeing the main CPU to spend more time on complex control calculations. At suitable points in the control cycle, the main CPU obtains new input readings from the TPU and presents new data for the TPU to calculate and schedule the output pulse timings.

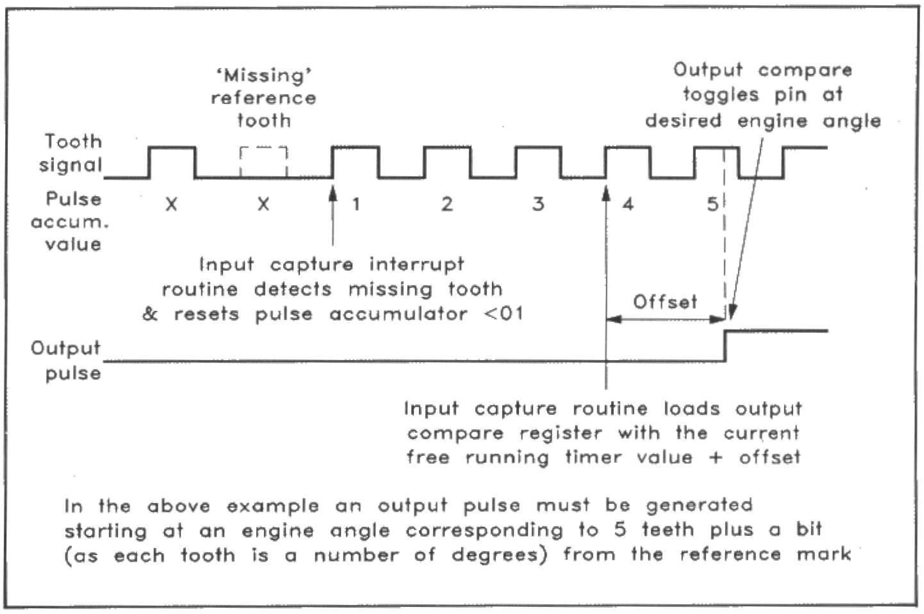


Figure 4. An example of output pulse timing.

Vehicle Alarms

The huge increase in car-related crimes in the 1980s has been paralleled by an equally large increase in the demand for car alarms. Originally based on simple logic circuits and triggered directly from interior light switches, the complexity of alarms has grown to try and match the skill of the potential intruder. Figure 5 shows the schematic of a typical sophisticated MCU-based alarm system. Using a microcontroller in this application provides a great deal of sophistication within a very low component count, allowing the alarm to be small and thus easily concealed. An MCU chosen for this job should have a 'low power' mode since the alarm must be powered up for long periods of time without the engine running. It should also be possible to 'wake' the device from this mode via several sources, so that a number of circuits can trigger the device into sounding the alarm. A simple 8 or 16-bit on-chip timer is also desirable to time the output audio/visual warning pulses and to reset the alarm after it has sounded for a set time – this is a legal requirement. The timer can also be used to arm the alarm after a defined period, if it is not armed via a remote control. For more details on an excellent microcontroller-based car alarm, the reader should refer back to the Maplin 'Compuguard' car alarm project (full details in Issues 40 (Oct-Nov'90) and 41 (Dec'90-Jan'91) of 'Electronics', with respective order codes XA40T and XA41U).

A.B.S.

The increased performance of everyday cars, along with their increasing numbers (and therefore greater density on the roads), has resulted in a continual improvement in braking performance. This trend has included the progression from all-drum braking, drum/disc braking and ventilated disc/drums, through to the all-disc braking systems found on todays higher performance cars. The most recent improvement has been the introduction of ABS. The Antilock Brake System (ABS) does not itself increase the braking capacity of the vehicle, but improves safety by maintaining optimum braking effort under all conditions. It does this by preventing the vehicle wheels from locking, due to over-application of the brakes, and thus maintains steerability and reduces stopping distances when braking on difficult surfaces such as ice.

ABS allows shorter stopping distances than with locked wheels, due to the friction or mu-slip characteristic of the tyre-to-road interface; as a wheel brakes, it slips relative to the road surface producing a friction force. A typical mu-slip curve is depicted in Figure 6. This shows that peak friction occurs at about 10 to 20% slip, and then falls to approximately 30% of this value at 100% slip (locked wheel). The aim of the ABS system is to control the braking force so as to stop the slip for any wheel exceeding this optimum value by more than an acceptable window.

At the heart of all ABS systems (except the all-mechanical system implemented by Lucas) is an electronic control unit (ECU) based around a powerful microcontroller. Figure 7 shows a block diagram of such a system. The solenoid valves that form part of the hydraulic modulator allow control of the pressure available to the individual wheel brake cylinders, independent of the force supplied by the driver via the brake pedal. These three-way valves can connect the brake cylinders to:

i) the normal master cylinder circuit, so that the braking pressure will be directly controlled by the driver.

ii) the return pump and accumulator in the hydraulic modulator, so that the pressure in the brake cylinders will fall as the fluid returns to the master cylinder.

iii) neither of the above two circuits, thus isolating the brake cylinder so that the pressure will be maintained at the value immediately preceding the move to this position.

The control for these valves is supplied via drive circuits from the output ports of the microcontroller.

The basis for all electronic ABS systems is the microcontroller's ability to determine the speeds of the individual wheels (although some front-wheel drive vehicles share a common speed sensor for both rear wheels). It does this via an inductive sensor and toothed ring that produce an output waveform, the frequency of which represents the speed of the wheel. This arrangement is almost

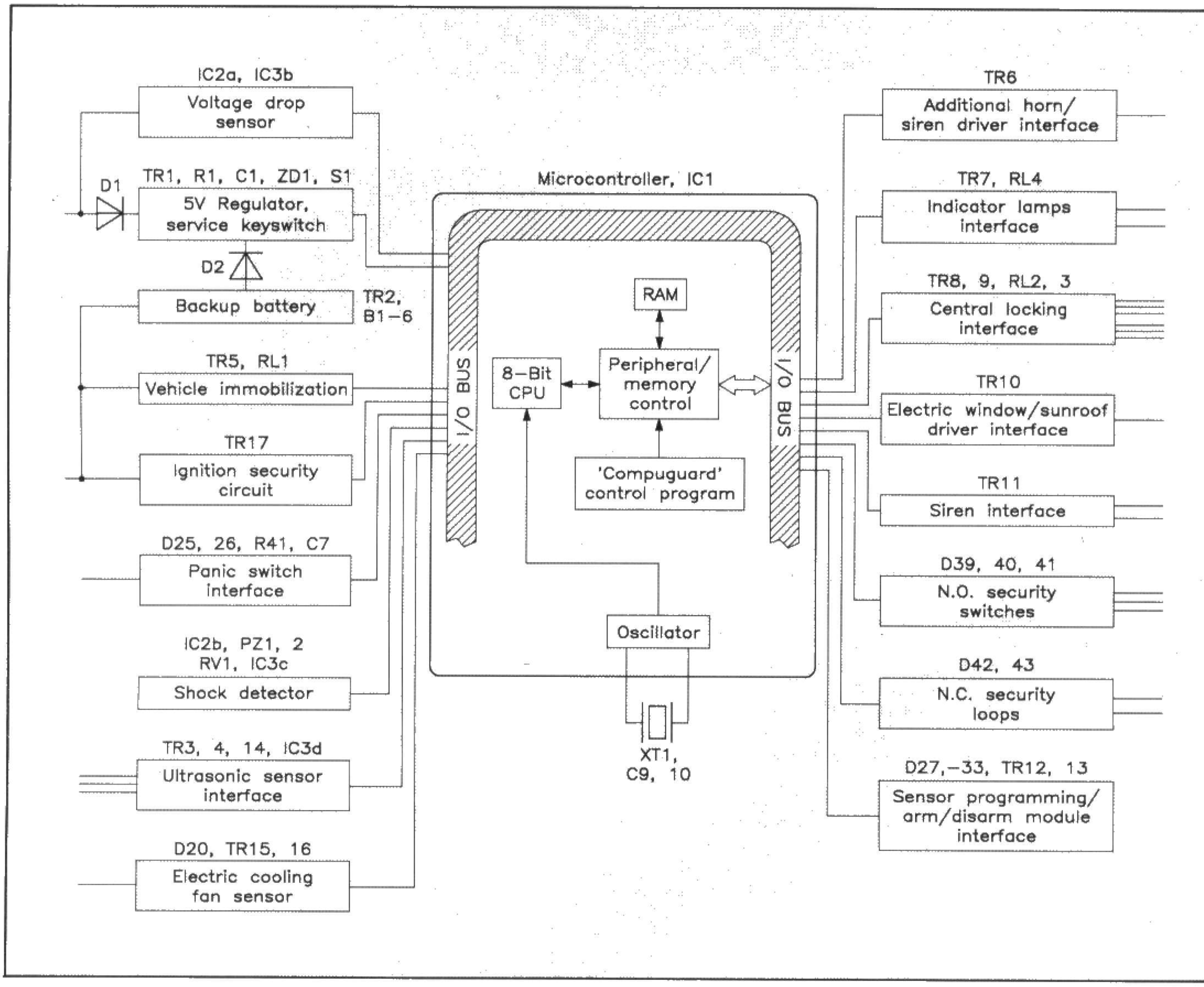


Figure 5. A μC-based Car Alarm system.

identical to the engine speed sensor discussed in the engine management chapter, except that since no angular position information is required there are no missing or extra teeth. It follows from this that the explanation previously given on determining engine speed also applies to determining wheel speeds in an ABS system.

In this case, there are around 50 to 100 teeth on the encoder ring, and this could result in a pulse frequency of 6000Hz when the vehicle is travelling well in excess of 100mph. Since there can be a speed sensor on each of the 4 wheels, a total of 24000 pulse edges have to be resolved every second. The solenoid valves in an ABS system typically have a response time of 10 to 20ms, and the microcontroller must be able to sample the inputs at least twice that often, to resolve lock-ups in 5 to 10ms. Put another way, the microcontroller must be able to determine 4 independent wheel speeds from 6000Hz signals within a 5ms window, and *still* have time to carry out processing on this data to determine the new valve states. These stringent timing requirements mean that ABS systems are the domain of high performance 16-bit microcontrollers that can respond quickly to interrupts from the timer system which is capturing the speed sensor edges.

So far it has been stated that the microcontroller in an ABS system must prevent the wheel-slip value from exceeding the optimum, and we have discussed how the μC measures the wheel speeds (angular velocity). However, it may not be clear how these wheel speeds are related to the slip values that the system is attempting to control. The slip of any wheel can be defined as the difference between the angular velocity of the slipping and non-slipping wheels, divided by the angular velocity of the non-slipping wheel. This makes sense and sounds quite simple, but for one problem; how to find a non-slipping wheel? The ABS algorithm searches for the fastest spinning wheel and uses this as the reference for calculating the slip values of the other wheels. If the slip value of a wheel is greater than the peak friction value by a certain margin (i.e. the wheel is heading towards a locked condition), then an ABS control cycle is executed on that wheel:

First the microcontroller will isolate the wheel brake cylinder from the brake circuit to prevent further pressure increase. It will then recheck the slip and acceleration values to determine if the wheel is still decelerating, and whether the slip value is still exceeding the desired value. If so, then the valve position is moved momentarily to the return position, reducing the braking effort on that

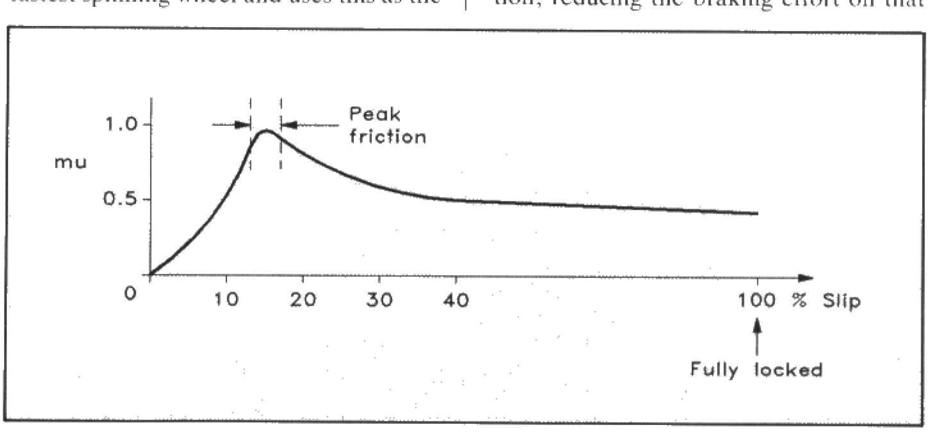


Figure 6. A typical mu-slip characteristic for the tyre-to-road interface.

wheel. This pulsed release of pressure is continued until the microcontroller detects that the wheel acceleration is positive, at which point it stops reducing the pressure, and reconnects the wheel cylinder to the brake circuit to prevent overshoot of the acceleration. This entire control cycle of holding/reducing/increasing brake pressure is repeated until the slip value for the wheel has been brought back into the acceptable window.

This is obviously a simplified explanation of how ABS works and the algorithms are in fact very complex and will vary from one ABS implementation to another. When you remember that this algorithm must be executed on all wheels in just a few milliseconds, it is not surprising that ABS is among the most demanding microcontroller applications. An important point worth discussing about ABS is that it is one of the most safety critical processor applications in existence. The consequences of a faulty ABS system could be potentially disastrous if the brakes were prevented from operating, or were applied erroneously. For this reason ABS manufacturers take great care in the safety aspects of the system design. It is not uncommon for two identical microcontrollers to be implemented, running the same software in parallel and continually checking each other via a communication protocol for any erroneous operation. Another solution to this problem is to have a simpler (lower cost) slave μC that acts as a 'watch-dog' for the main ABS microcontroller. This slave device is programmed to monitor the major activities of the master μC and it has the ability to shut down the ABS system if a fault is detected, thus reverting full braking control to the driver.

A subject worth mentioning here is traction control. Traction control is a fairly recent development and can be thought of as applying ABS in reverse. The idea of traction control is to prevent wheel-slip due to excess power on loose surfaces by applying a braking force to the slipping wheel (note that traction control is only implemented on the driven wheels). This feature is a natural progression for ABS, as all the necessary components and measurements required for traction control are inherent in the ABS system – except some means of applying a braking force when the driver is not depressing the brake pedal. This is usually achieved via an electric pump arrangement. With the considerable improvement in safety provided by ABS, there can be little doubt that the next few years will see this system becoming more popular, possibly becoming a standard feature on all but the lowest cost cars.

The Future

Hopefully this series will have given the reader some insight into the fascinating and challenging applications for microcontrollers in automotive applications. It has, of course, been impossible to cover all of the applications listed in Part 1 of this article, or even to cover some of those we have in great technical depth (engine management or ABS could each fill a text book), but the selection chosen has shown just how varied in complexity the automotive microcontroller application can be. As a finishing thought, it may be worth pondering what the future holds for electronics, and particularly microcontrollers, in cars. Perhaps the next major advance, one which all the major vehicle manufacturers and standards bodies are working on, is the multiplexed wiring system. As the electrical content of vehicles escalates ever higher, the weight and cost of all the interconnecting cables is becoming a major concern, and the number of electrical connectors poses a reliability problem – most vehicle breakdowns are due to electrical faults. The concept of the multiplexed wiring system is to use a very high performance serial communications network between intelligent and semi-intelligent modules stationed at strategic points around the vehicle. This means that only power and the serial link need be distributed about the car – all the loads have short connections to the nearest intelligent sub-module. The possibilities of this system are enormous; the engine management system could 'talk' to the electronic gearbox controller and to the ABS/traction control system. No longer would turning on your lights simply connect power directly to the bulb – it would signal one unit to send a command to another unit, instructing it to turn on the bulb using a 'Smart Power' device. This scenario is not fantasy, it is going to happen and since the microcontroller has a place at the heart of every one of these intelligent modules, it is safe to say that its future in the automotive market is very secure indeed.

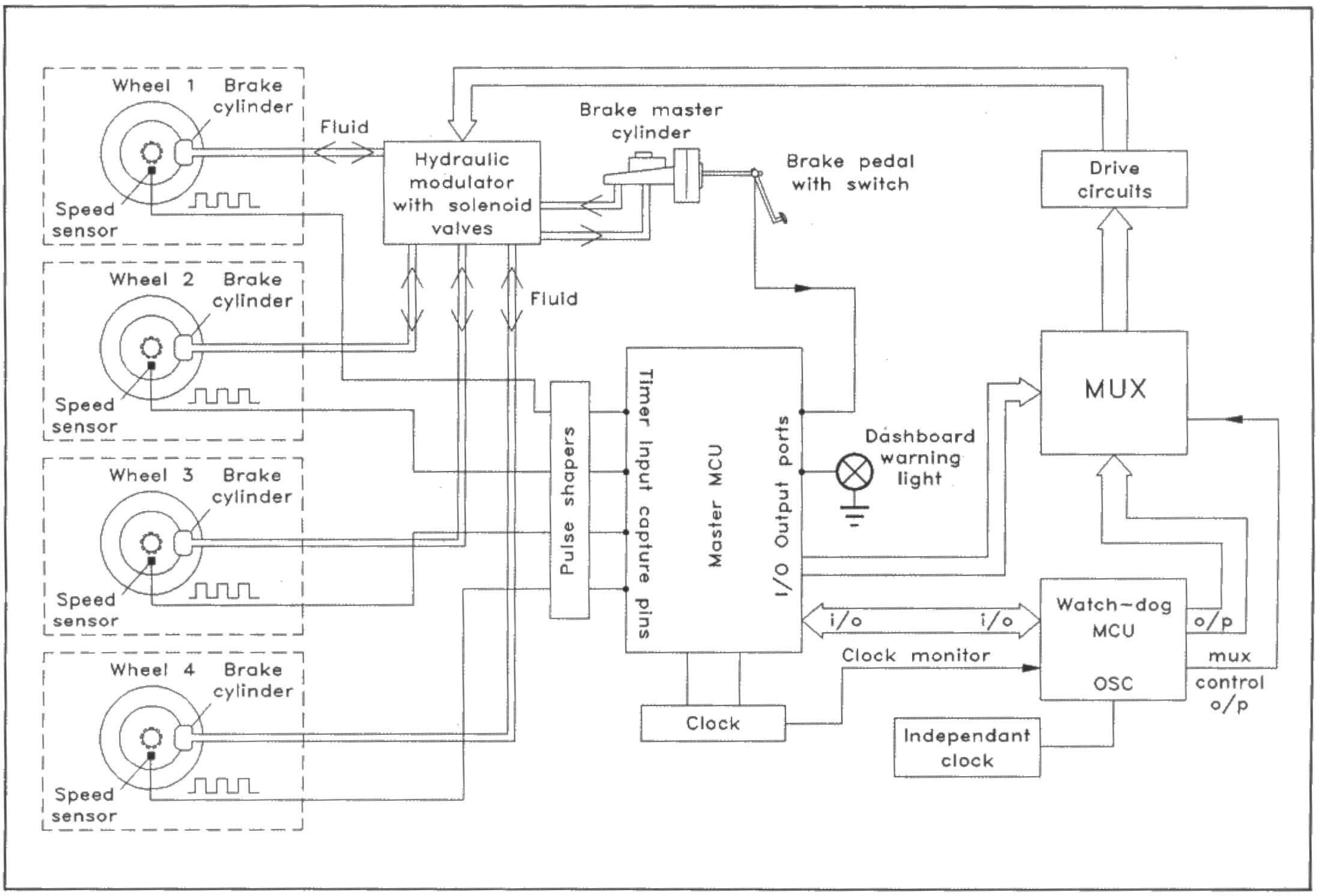
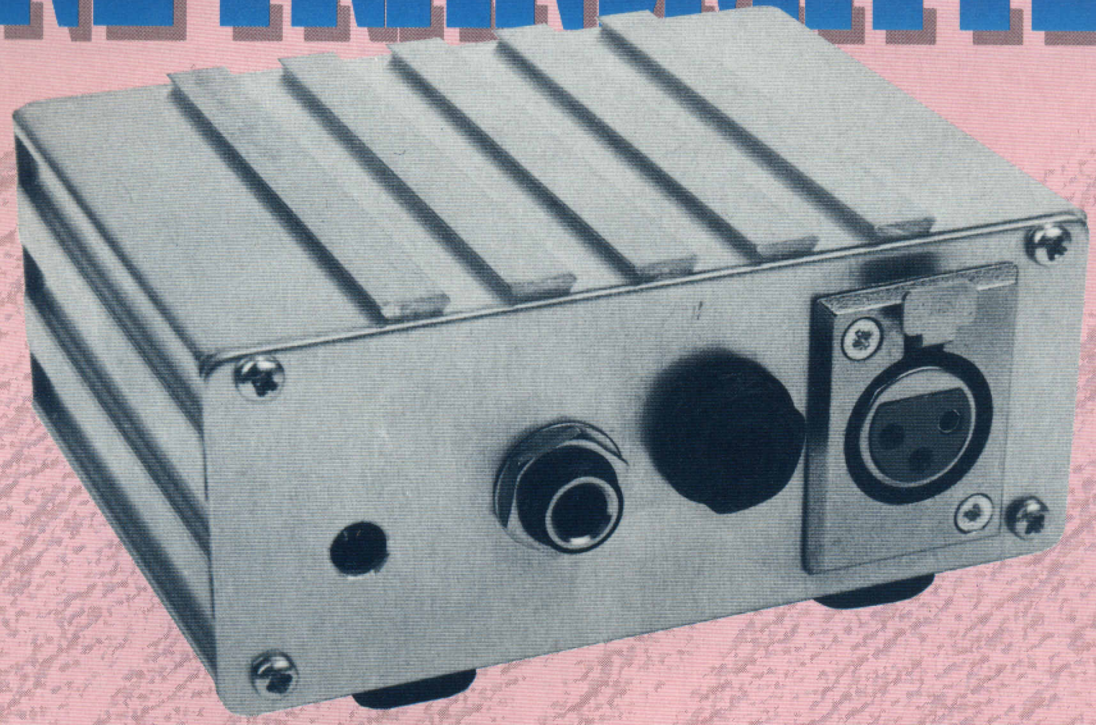


Figure 7. Block diagram of an electronic ABS system.

AUDIO BALANCED LINE TRANSMITTER



by Alan Williamson

Balanced line systems were originally developed to overcome the hum and noise pickup problems that inevitably crop up with unbalanced (single-ended) cables over long runs. The situation does not exist when using a balanced line because any externally introduced noise component will be equally induced on both the in-phase and out-of-phase signal lines, keeping the signal differential voltage the same, which effectively cancels any common-mode noise, see Figure 1.

An unusual application for a balanced line transmitter is to use it as a phase splitter at the input of a stereo amplifier, or two identical mono amplifiers, allowing the two channels to be used in 'bridged' mode (if they aren't already). The loudspeaker would then be wired across the left + (plus) output and the right + (plus) output. In the case of two mono amplifiers, or separate power supplies in the stereo amplifier, the two speaker – (minus) outputs should be commoned together, as in Figure 2. However, it should be pointed out that not all amplifiers can be used in this way. These include, for example, amplifiers already wired in a bridged configuration, and certain valve amplifiers.

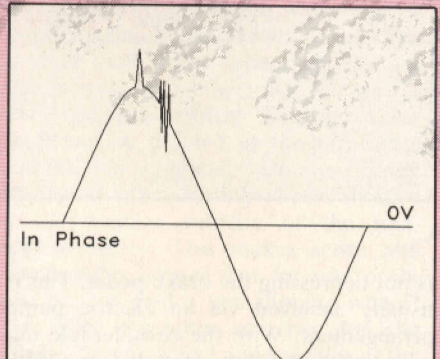


Figure 1. Balanced signal and noise.

Power Supply Circuit

Referring to Figure 3, it can be seen that the circuit is supplied with power only when a jack plug is inserted into the unbalanced input jack socket (SK1). The power can be derived from a mains adaptor via the power socket (SK3), or from two PP3 batteries when used in portable applications. The power socket disconnects the battery supply when a mains adaptor is used, and diode D1 will prevent damage to the circuit from accidental reverse-polarity connections to the mains adaptor.

Transistors TR1 and TR2, in conjunction with associated components R3/R4 and C12/C13, form supply filters – tantalum capacitors are ideal for this application.

The signal circuit requires a split-rail power supply (+V,0V,–V), and this is achieved using a potential divider (R6 & R7) to generate the half-supply reference for the non-inverting input of IC3, which is configured as a unity gain buffer, providing current gain.

Signal Circuit

With reference to Figure 4, the signal enters the circuit via input jack socket

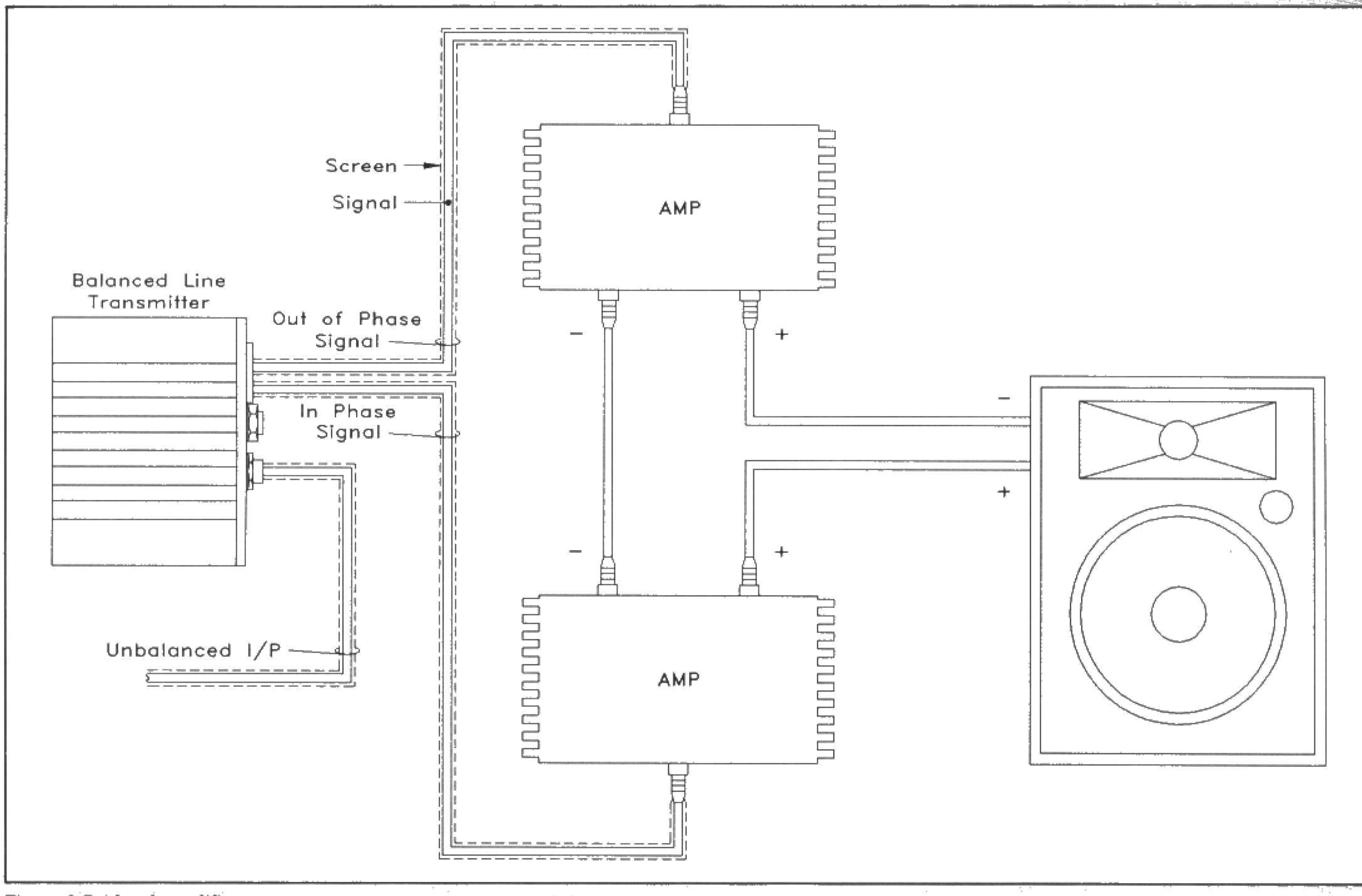


Figure 2. Bridged amplifier.

(SK1), and is AC-coupled by C1 and C2, to R1. R1 is the input terminating resistor, which determines the input impedance and, in conjunction with R2 and C3, limits the upper frequency response. This begins to roll off at around 80kHz.

IC1 is configured as a unity gain buffer, providing plenty of drive via C4 and C5 to SK4, which is the 'fold-back' output used for monitoring purposes.

IC2 is an SSM-2142 purpose-designed cross-coupled balanced line driver, which is capable of driving very long cables, with capacitances of up to 160nF, into a 600Ω load. The IC has two sets of outputs; +Force (+F), +Sense (+S) & −Force (−F), −Sense (−S). For each of the outputs, the Force and Sense would normally be linked together.

The Sense outputs are used where large common-mode DC offsets are encountered on the cable, or for ensuring an optimum noise rejection performance by avoiding differential offset error sources. This is achieved by fitting the optional capacitors C6 to C9 in place of LK1 and LK2. The offset error becomes an important factor only when extremely long cable distances (hundreds of metres) are involved, and should not be a problem under normal conditions.

The +S & −S outputs of IC2 have been made available on PCB pins for those of you who wish to use a 5-wire system (2 signal, 2 remote sense, 1 screen); C6 to C9 and LK1,2 are not fitted on the PCB in this application.

Construction

First of all, if you are new to the hobby, read the Constructors Guide supplied with the kit. The Guide contains some useful information on component identification, soldering and constructional techniques.

Begin construction with the smallest components first, working up in size to the largest; use the component off-cuts for the eight links. The board legends are shown in Figure 5 for your reference. A little extra care must be taken with the polarised devices. The PCB pins are inserted from the track side, and you may prefer not to fit the PCB pins (+F, −F, +S, −S, 0V) for the output XLR socket. It is possible to DC-couple the input, by fitting a link in place of C1 and leaving out C2. This will improve the performance slightly, but first of all please check that there is no DC offset at the output of the equipment intended to drive the balanced line, otherwise the circuit may be damaged.

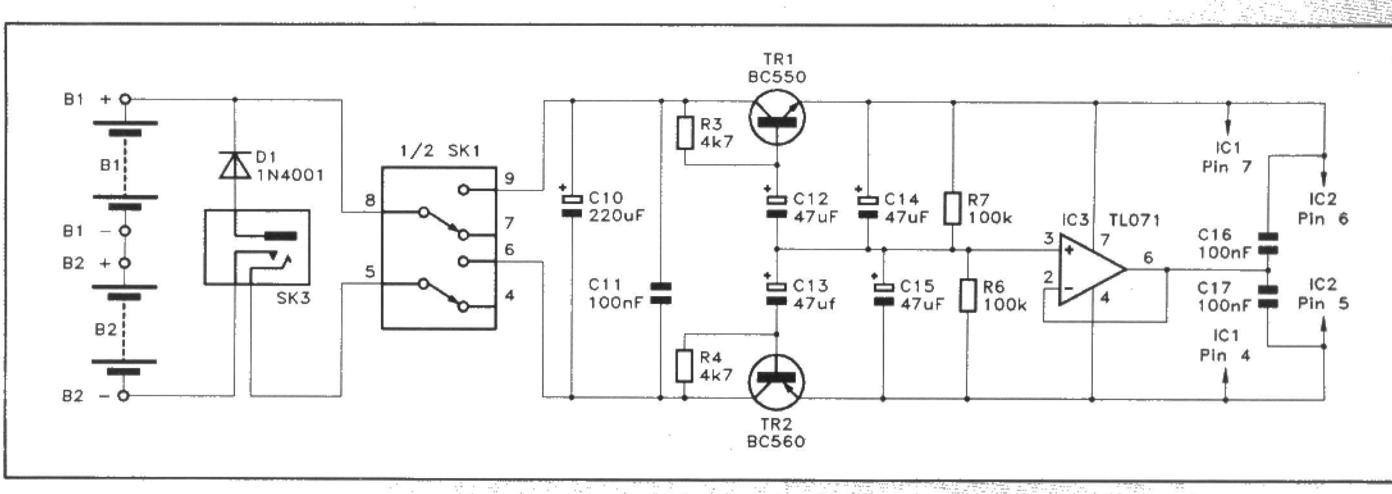


Figure 3. Power supply circuit diagram.

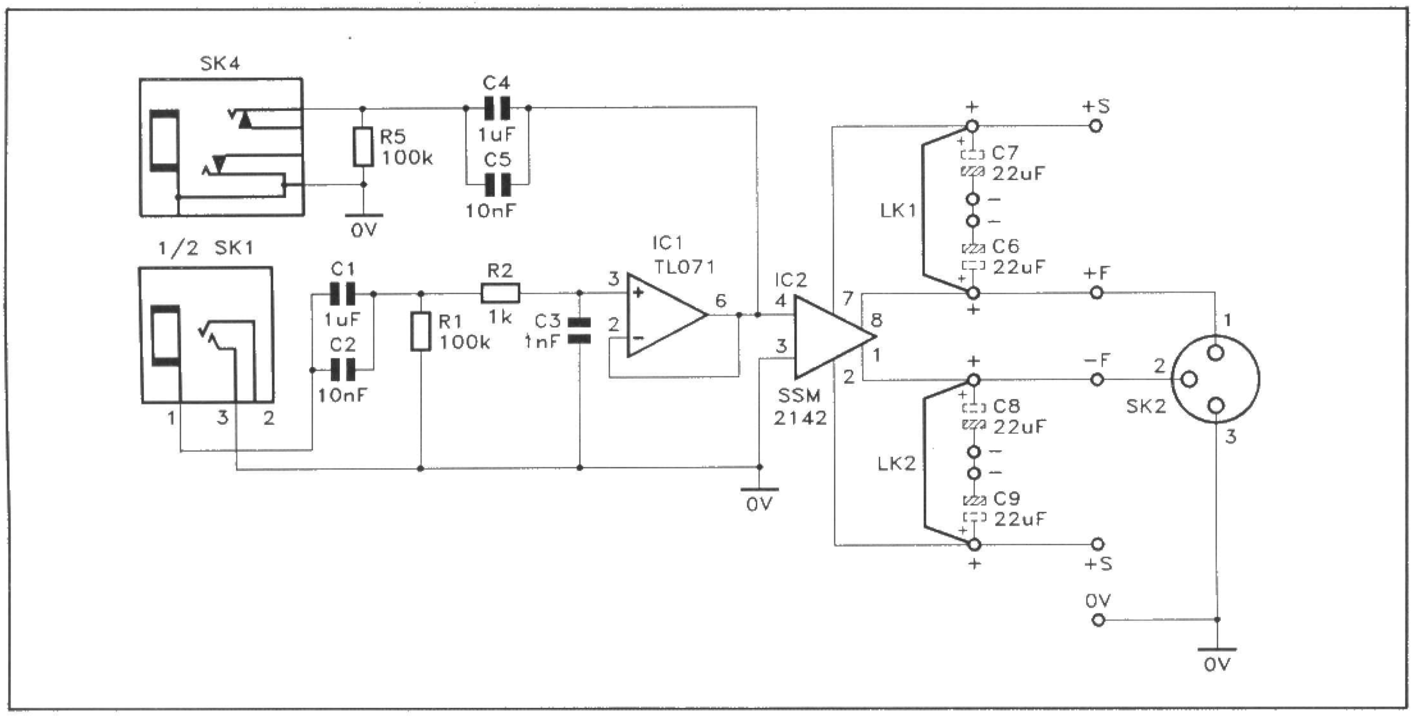


Figure 4. Balanced amplifier circuit diagram.

Testing

To test the balanced line transmitter, some equipment is required consisting of: a power supply (+9V min to +35V max, an unregulated mains adaptor would suffice e.g. XX09K); a signal source (e.g. audio oscillator, guitar, keyboard, cassette player etc.); and an oscilloscope, or amplifier with an unbalanced input (if you have a guitar you will probably have a guitar amp).

First, apply power to the circuit via a mains adaptor or batteries, then feed a signal (up to 1V rms at any audio frequency between 20Hz and 20kHz, as long as you can monitor it) to the input socket SK1 from your oscillator/signal source (inserting a jack plug into the input socket (SK1) will power up the circuit). Connect a second jack lead to the 'fold-back' output socket (SK4), and monitor the signal on your oscilloscope/amplifier; the signal will be in-phase and almost equal in amplitude to the signal source, although some signal will be lost across R2. For the next test, connect the +F & 0V pins of the XLR socket to your oscilloscope/amplifier, and monitor the output which will also be in phase and equal in amplitude to the signal present at SK4. Repeat the test with the −F & 0V pins; this time the signal will be out-of-phase, but with the same amplitude. The module has now been tested, and is ready for use after being boxed.

WARNING! The balanced line transmitter must be powered up before connecting to a 'live' input; any input offset voltage present at the next stage could turn on the output devices of IC2, which could result in this component being permanently damaged.

Housing the Module

Remember, SAFETY FIRST! Goggles should be worn at all times when power tools are being used.

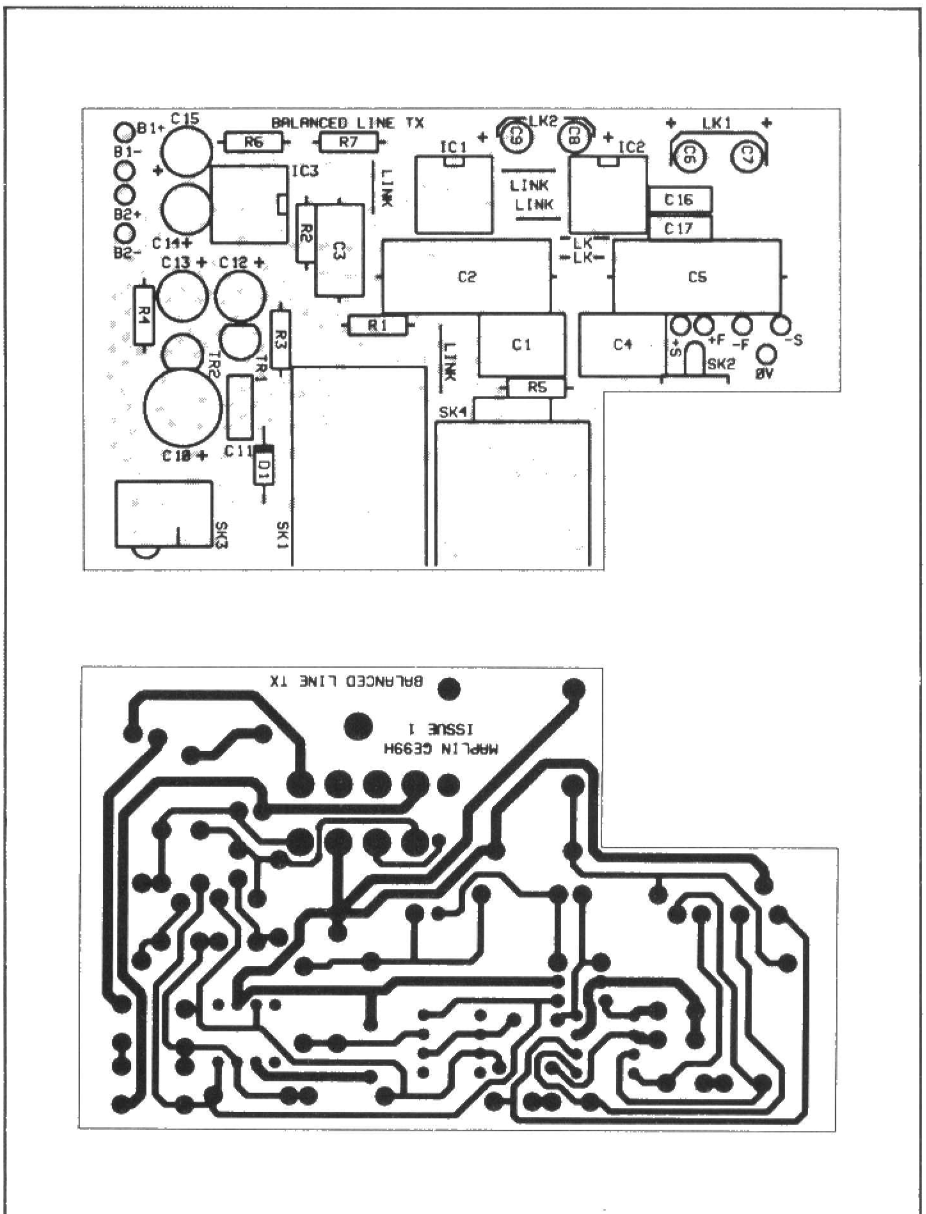


Figure 5. PCB legend and track.

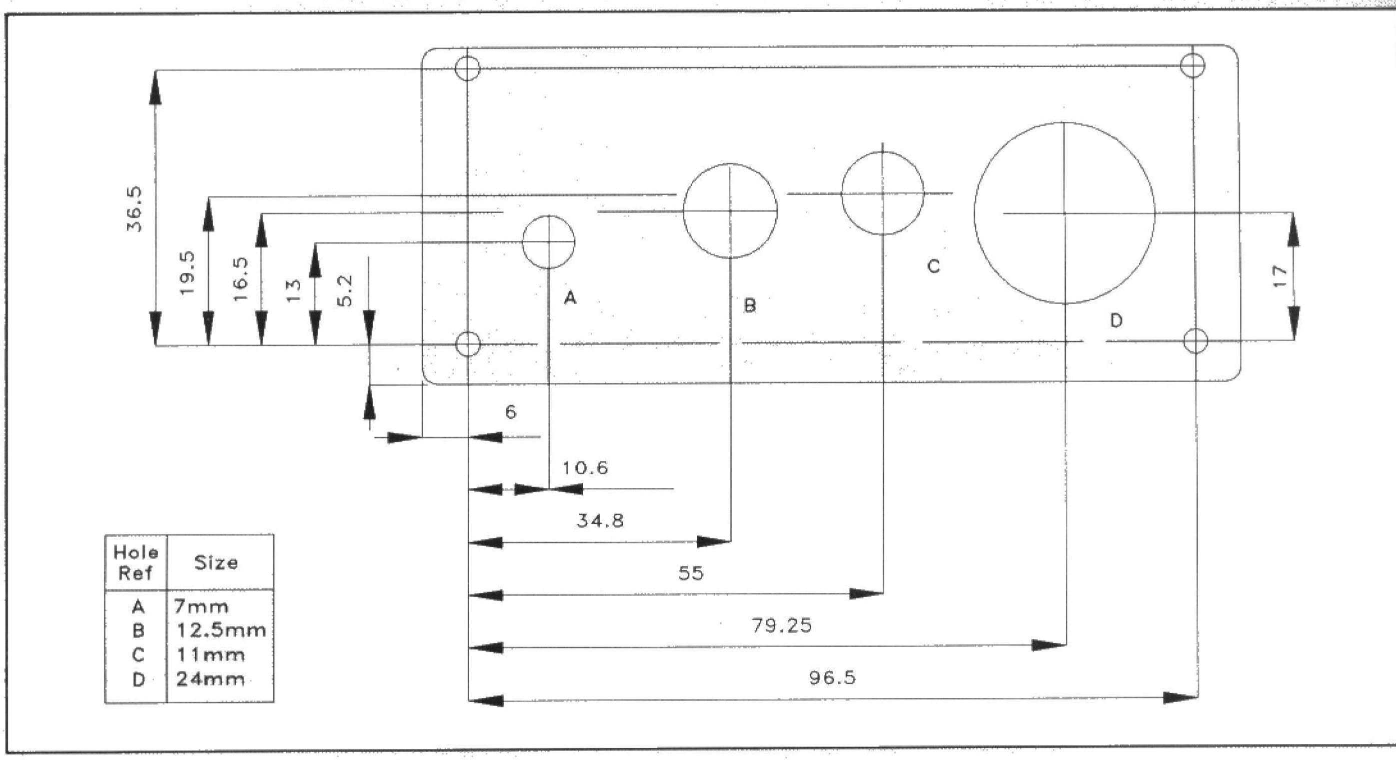


Figure 6. Box front panel drilling details.

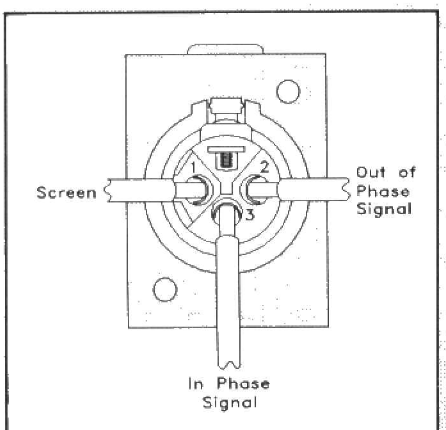


Figure 7. XLR socket wiring.

We strongly recommend the use of the optional box, which will provide a high degree of screening in noisy environments, as well as being a good sturdy home for the PCB.

Figure 6 shows the optional box front panel drilling details. Mark out the holes to be drilled first; the easiest way to make the large hole for the XLR socket is to drill a series of smaller holes around the inside of the circle (that you have marked out previously), and join the holes together using a 'rat's tail' needle file (a small round tapered file). Drill out the rest of the holes in the front panel to the sizes given.

Fix the XLR socket to the front panel using two M2·5 10mm countersunk posi-screws, two M2·5 shakeproof washers and two M2·5 nuts. Cut three 25mm lengths of the supplied wire, solder the three pieces of wire to the XLR socket, then to the appropriate PCB pins as shown in Figure 7. Attach the PCB to the front panel using the jack socket nuts, and remove the back panel of the box. Attach half a quickstick pad on top of IC1 and the other half on IC2, this will be the position for the battery, B2. Fit the B2 battery clip

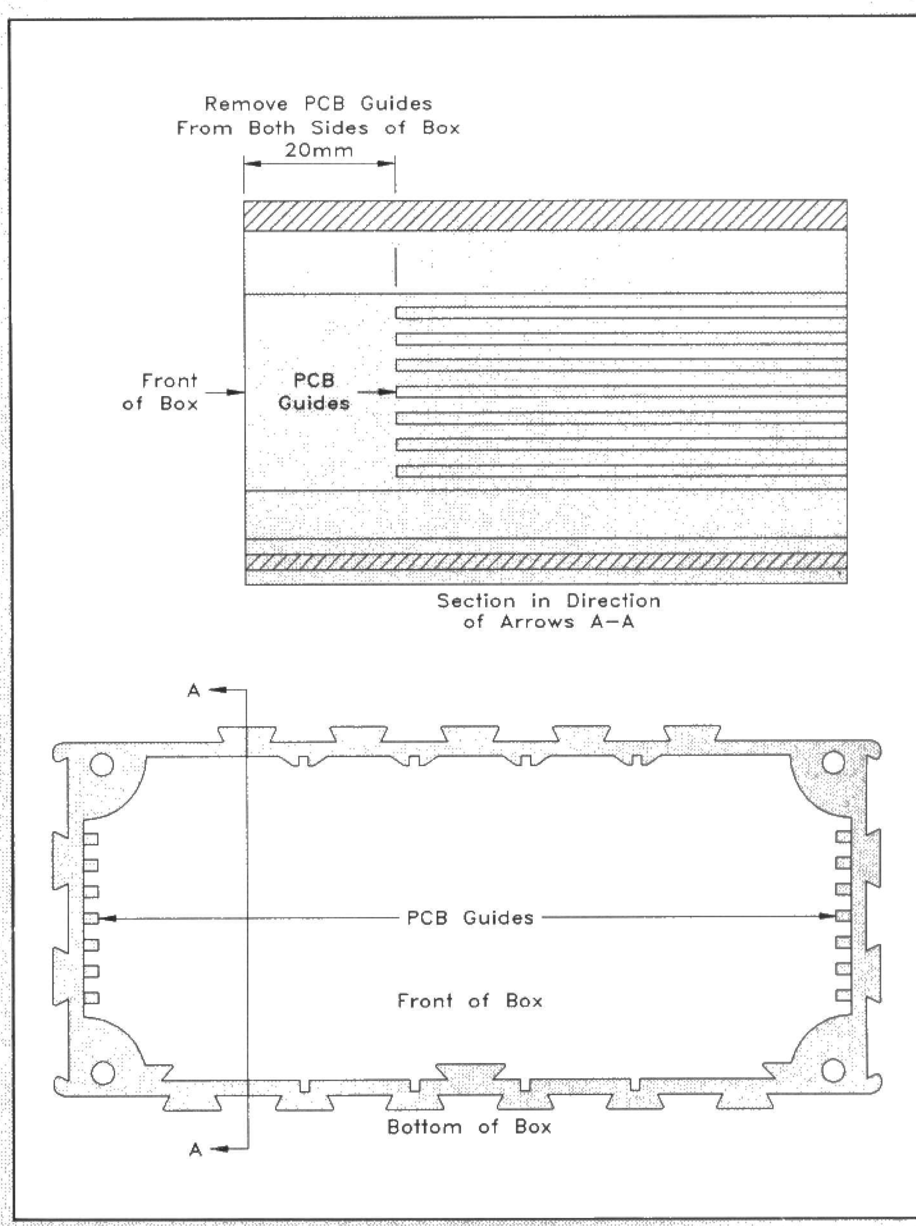


Figure 8. Box modification.

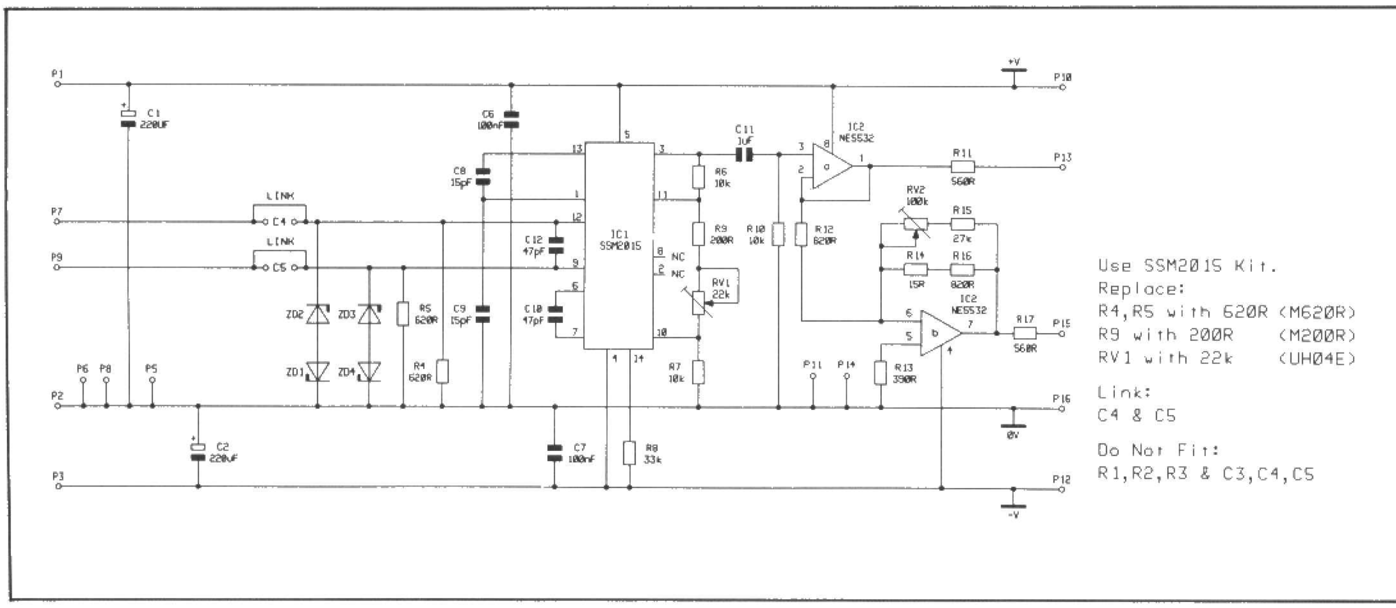


Figure 9. Modified SSM 2015 circuit diagram.

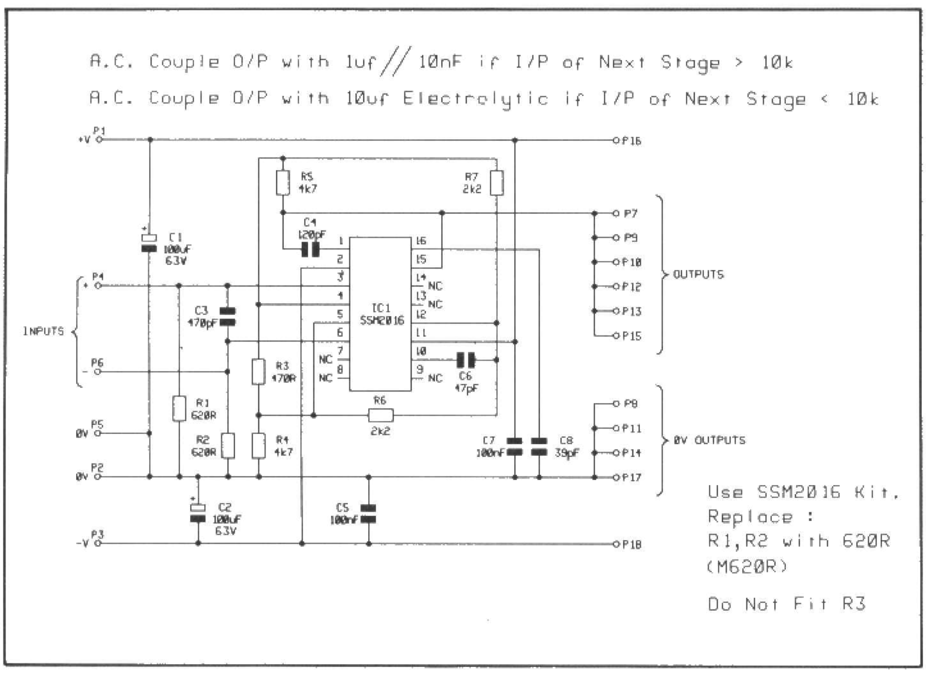


Figure 10. Modified SSM 2016 circuit diagram.

to a PP3 battery, which should be placed onto the quickstick pads, pushing down to make sure that it is firmly secured. Slide the PCB into the box and attach the B1 battery clip to a second PP3 battery; this second battery is attached to the back panel also using quickstick pads. Screw the back panel on and the unit is ready for use. If you do not find this a satisfactory arrangement for the batteries, a little more work on the box is required. Figure 8 illustrates the modification to the box allowing the batteries to sit side-by-side in the rear of the box. I used a mini drill and a 1·4mm burr to do the job; you will need to have patience as this takes quite some time.

Balanced Line Receiver

There are two projects that would make ideal receivers; these are the SSM-2015/6 Data Files (published in 'Electronics' issues 39/41; Aug-Sept '90 & Dec '90-Jan '91 respectively), although some of the component values will need to be

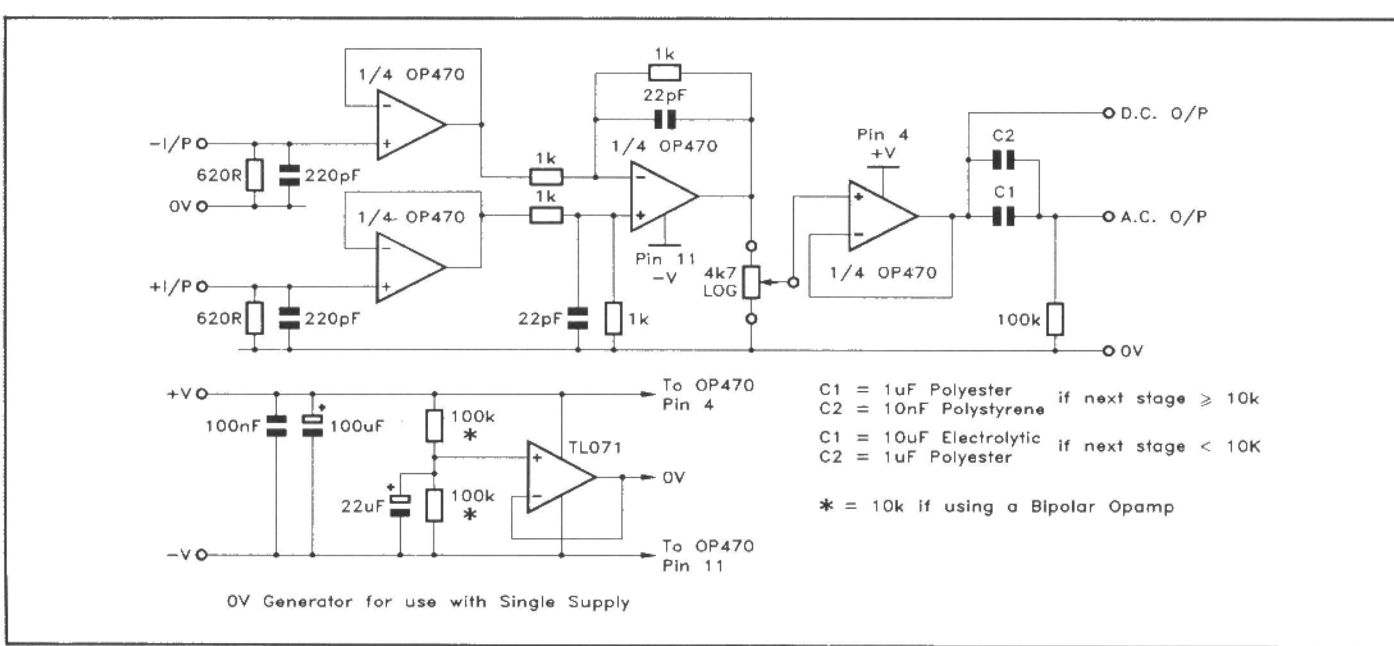
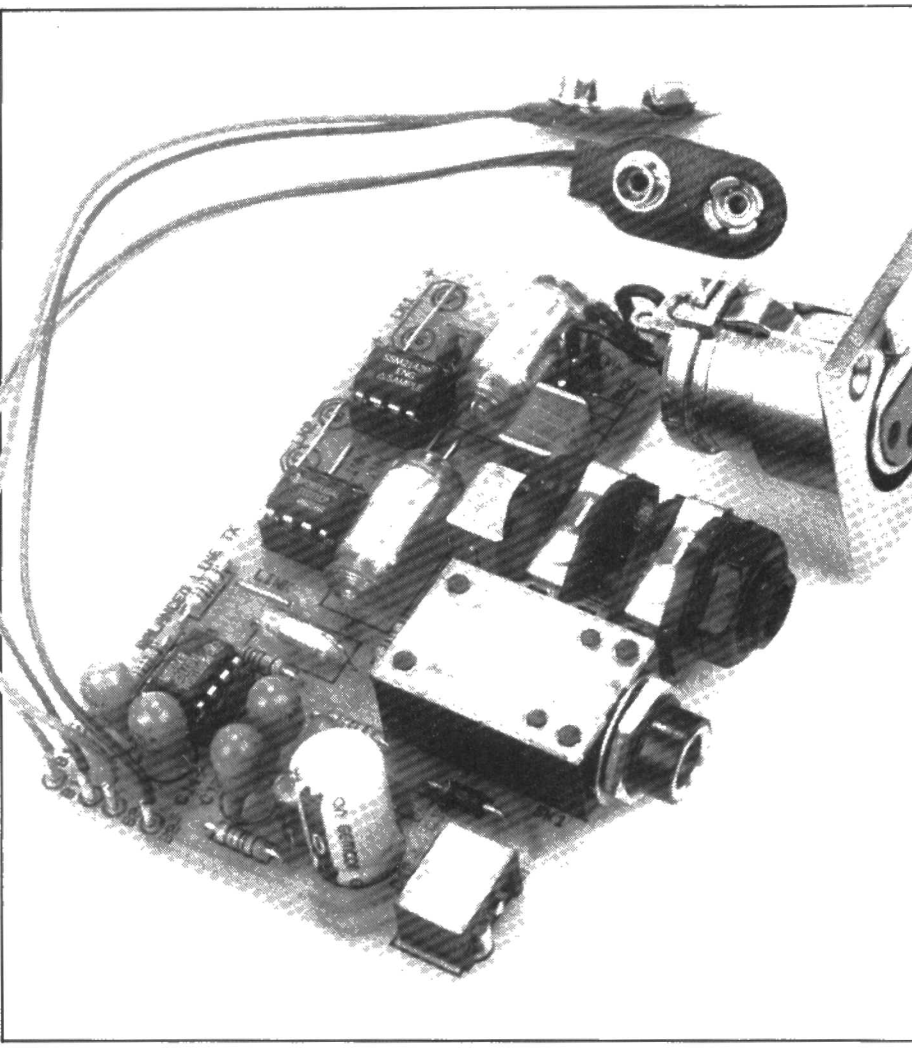


Figure 11. OP470 receiver circuit.



changed. The modified circuit diagrams of the SSM-2015/6 Data Files are shown in Figures 9 and 10.

The component changes to the SSM-2015 module are as follows: resistors R1,2,3 and capacitors C3,4,5 are not fitted; wire links are fitted in place of C4 and C5. In addition, the values of the following components are altered: R4 and R5 to 620Ω; R9 to 200Ω; and VR1 to 22kΩ. The value of VR1 determines the gain of the IC; the higher the value of VR1, the lower the gain (minimum 3·5).

The SSM-2016 requires minimum alteration. Change R1 and R2 to 620Ω, and R3 to 22kΩ. The gain is approximately 3·5, and can be increased by reducing the value of R3.

An alternative to the SSM-2015/6 kits would be to use an OP470 quad op-amp, as shown in Figure 11; the output buffer could be configured as a gain stage, or used as the 0V (half-supply) generator in single-supply applications.

Prototype Specification

Supply voltage:	9V minimum, 35V maximum
Quiescent current	
@ 9V:	8·2mA
@ 35V:	9·5mA
Maximum input signal	
@ 9V:	1·4V rms
@ 35V:	10V rms
Frequency response	
@ −3dB:	1·5Hz to 100kHz

AUDIO BALANCED-LINE DRIVER PARTS LIST

RESISTORS: All 0·6W 1% Metal Film			
R1,5,6,7	100k	4	(M100K)
R2	1k	1	(M1K)
R3,4	4k7	2	(M4K7)
CAPACITORS			
C1,4	1µF Poly Layer	2	(WW53H)
C2,5	10nF Polystyrene	2	(BX92A)
C3	1nF Polystyrene	1	(BX35Q)
C10	220µF 35V PC Electrolytic	1	(JL22Y)
C11,16,17	100nF Ceramic	3	(BX03D)
C12,13,14,15	47µF 16V Tantalum	4	(WW76H)
SEMICONDUCTORS			
D1	1N4001	1	(QL73Q)
TR1	BC550	1	(UL49D)
TR2	BC560	1	(UL50E)
IC1,3	TL071CP	2	(RA67X)
IC2	SSM2142	1	(UM54J)
MISCELLANEOUS			
SK1	Sw PCB Stereo Jk Skt	1	(FJ87U)
SK2	XLR Chassis Socket	1	(BW90X)
SK3	PCB 2·5mm DC Pwr Skt	1	(FK06G)
SK4	Mono PCB ¼in. Jk Skt	1	(FJ00A)
	DIL Socket 8-Pin	3	(BL17T)
	PP3 Clip	2	(HF28F)
	Pins 2145	1Pkt	(FL24B)
	Black Bell Wire	1	(BL85G)
	PCB	1	(GE99H)
	Instruction Leaflet	1	(XT29G)
	Constructors' Guide	1	(XH79L)
OPTIONAL (Not in Kit)			
C6,7,8,9	22µF 16V Tantalum	4	(WW72P)
	Box CCN80	1	(YN50E)
	Gasket CCN80	1	(FE41U)
	Pozi Screw M2·5 x 10mm	1Pkt	(JC68Y)
	Steel Nut M2·5	1Pkt	(JD62S)
	Isoshake M2·5	1Pkt	(BF45Y)
	Battery Alkaline K9V	2	(FK67X)
	AC Adptr Unreg 300mA	1	(XX09K)
	Quickstick Pads	1	(HB22Y)
	Rubber Foot	1	(XR93B)

The Maplin 'Get-You-Working' Service is available for this project, see Constructors' Guide or current Maplin Catalogue for details.

The above items (excluding Optional) are available as a kit, which offers a saving over buying the parts separately.

Order As LP49D (Audio Balanced Line Driver Kit) Price £14.95

Please Note: where 'package' quantities are stated in the Parts List (e.g. packet, strip, reel, etc) the exact quantity required to build the project will be supplied in the kit.

The following new item (which is included in the kit) is also available separately:

Balanced Line Tx PCB **Order As GE99H Price £2.95**

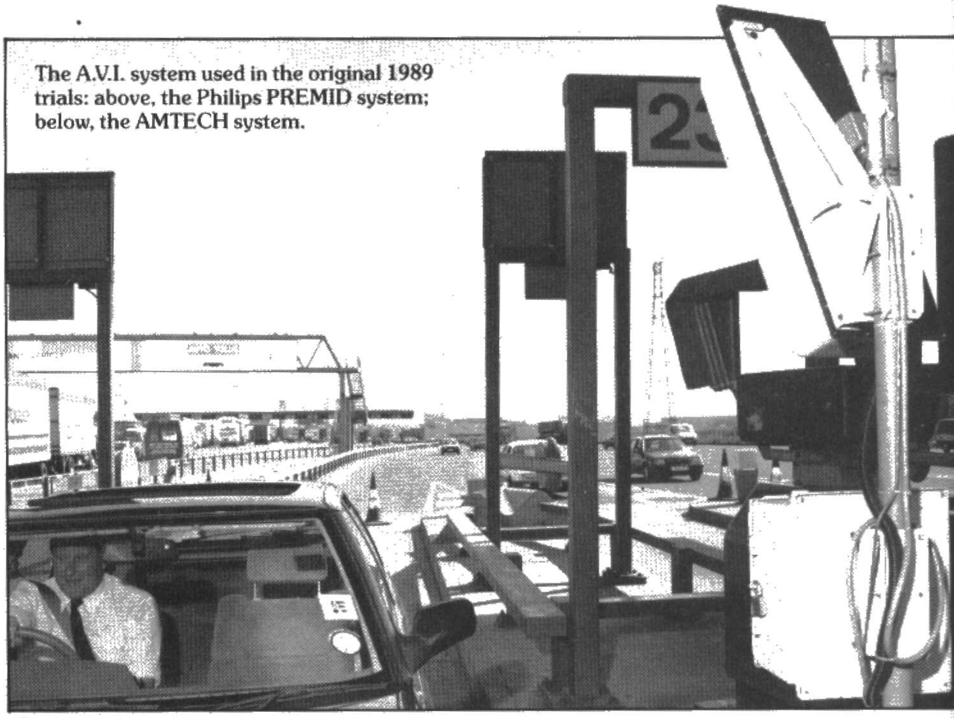
A New Landmark for the Thames continued from page 17.

used antennae mounted on the side of the lane to communicate with a uniquely-coded identification 'transponder' tag, positioned in the rear quarterlight of the vehicle. The system, which operated at a frequency of 2·4GHz, used software specifically adapted for the trial. Amtech, however, used an antenna positioned towards the exit of the toll lane at a height of 2·5 metres, looking downwards along the lane. This communicated with a tag fixed to the windscreen of the vehicle. The system operated at a frequency of 888MHz, and used specific A.V.I. software.

The tests were successful, both systems improving collection throughput. There were no problems generated by crosstalk between lanes, or interference caused by electrical systems (e.g. poorly suppressed alternators fitted to vehicle engines). In addition, both systems proved to be completely compatible with the existing toll collection arrangement. The vehicle discrimination abilities (with and without barriers), the effect of different ground loop responses, and the susceptibility to RF interference from vehicle equipment and mobile communication systems (e.g. CB radio and cellphones) were also tested. Again, both sets of equipment scored well. Any problems discovered were easily overcome by slightly relocating barriers, loops and A.V.I. antennae from their original trial positions. Customer reaction was also good and the barriers, seen as an essential anti-fraud measure, will remain.

Final Choice

As a result of these trials, Dartford River Crossing Limited has awarded French company CSEE the £2m contract to install the A.V.I. system. In between the trials and the placing of the contract, a version of PREMID manufactured by SAAB Automation was chosen as the basis of the Bridge A.V.I. system. The final choice was made from a total of eight, submitted by Consulting Engineers Mott MacDonald for the contract. As with the trials, the CSEE PREMID-based system will work by transmitting to a unique identification tag mounted behind the vehicle window. When 'cleared', the computer system will then debit the customer's account and raise the barrier. The system will operate at a slightly modified frequency of 2·45GHz. In order to ensure the necessary 'elliptical' pattern of detection, two antennae will be used. One will be mounted 1·5m from the road surface (to deal with transponders in cars and vans) while the other will be mounted 2·2m from the roadway (to ensure coverage for large vehicles such as coaches, HGVs etc.). The system will use the existing loops but there will also be an extra loop placed in the traffic lane to facilitate faster processing. This should mean that an approach speed of 20 mph can be accommodated. As a result, a high speed (0·8 seconds) barrier lift sequence will be incorporated into the A.V.I. payment routines.



The A.V.I. system used in the original 1989 trials: above, the Philips PREMID system; below, the AMTECH system.

The identification tags will be of the same size as a tax disc, and the system will work upon a debit basis. Each will be unique to the vehicle in which it is fitted, and either pre-payment or a valid credit account will produce the debit entry. It is estimated the signal will be such that the vehicle need only slow to 20 mph, subject of course to traffic conditions. This means that there need be no stopping, particularly as there will be no pass or smart-cards to move around.

All approach lanes will be equipped with A.V.I., with initially one 'fast' lane equipped only with A.V.I. equipment. Judgment and take-up will determine how many more toll-booths will be equipped solely with this system. The Dartford Tunnel (used for the return journey) will also be equipped with A.V.I. equipment at each booth, and the number of A.V.I.-only lanes will be kept proportionally the same as that of the Bridge. The need for a financial incentive has not been lost on the operating company, who have still to reveal pricing policy. It is clear that, as with the current pre-payment arrangements, there will be a recognition of the savings made in the pricing of A.V.I. The company are aiming for 30,000 to 40,000 A.V.I. collections per day. This, they hope, will eventually lead to A.V.I. being the collector of 50% of the tolls. Other A.V.I. systems currently operate in France, Italy and in much of the United States (including the largest current operation, which is installed in 12 booths of a New Orleans facility).

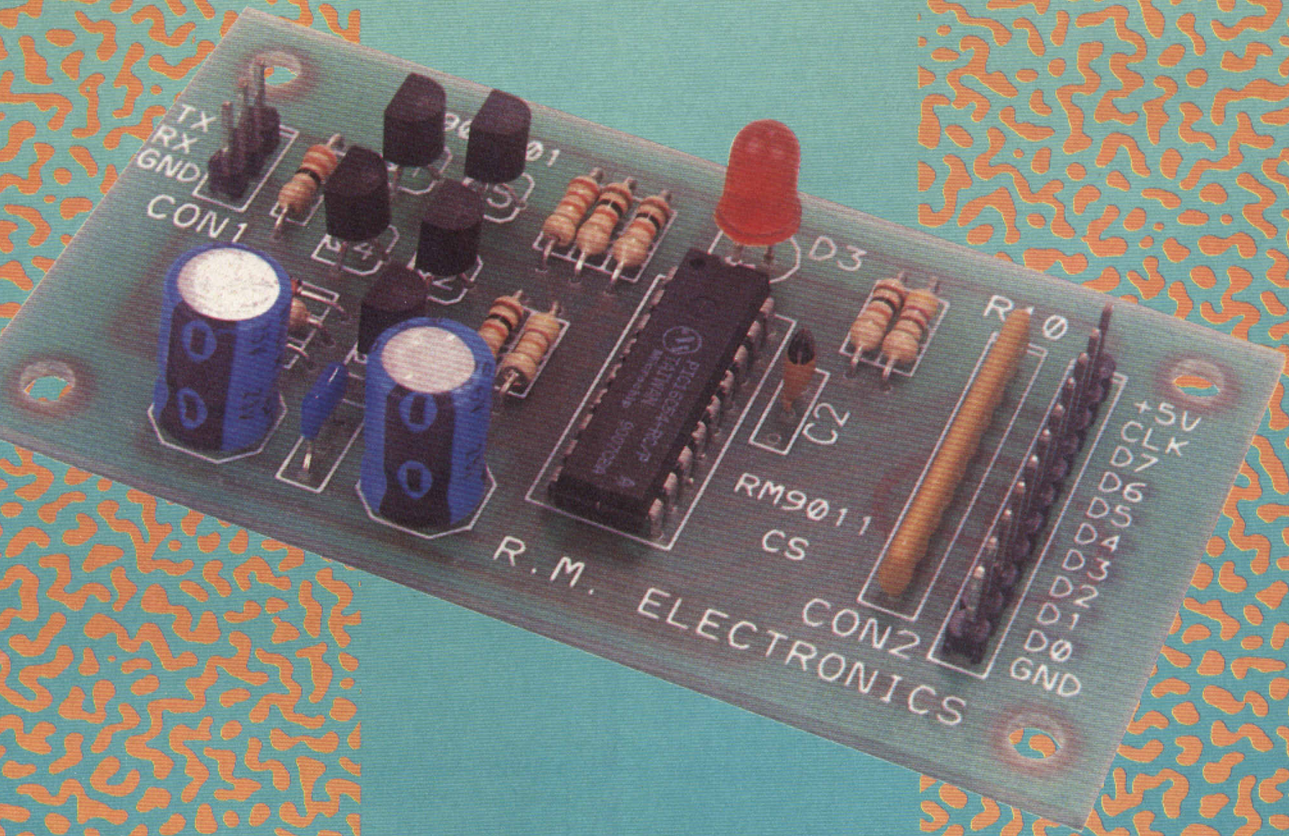
As well as collecting the money A.V.I. will produce statistical and audit data. It will also pin-point the whereabouts of a specific vehicle, at a certain time and place. It will be able to analyse traffic flows both by types and numbers of vehicles. Most of all, it will start to accustom the British motorist to having electronic payment systems both in his car and at the roadside. From there, it will be only a short step to using the same technology for comprehensive road pricing. But, that is another story. For now, let the new 'Landmark for The Thames' be proud of the fact that it has not only created a financial and political stir, but it has also introduced new and sophisticated electronics into yet another part of our daily lives.

Acknowledgments

Thanks to Paul Emberley at Dartford River Crossing Limited for his very considerable assistance, also Anne Buttfield and Ron Holmes of the Mott MacDonald Group.

RS232 to 8-bit DIGITAL I/O CONVERTER MODULE

Reviewed by Tony Bricknell



FEATURES

- ★ Each I/O line individually configurable as input or output
- ★ Byte or bit read and write
- ★ Configuration can be altered on-line through the RS232 interface
- ★ Single 5V DC supply voltage
- ★ I/O lines are TTL and CMOS compatible
- ★ On-board CMOS microcontroller

APPLICATIONS

- ★ Digital I/O expansion of any computer with an RS232 interface
- ★ Computer-based process control and automation
- ★ Capture of digital signals, switches, detectors, etc.
- ★ Computer control of relays, motors, pumps, etc.

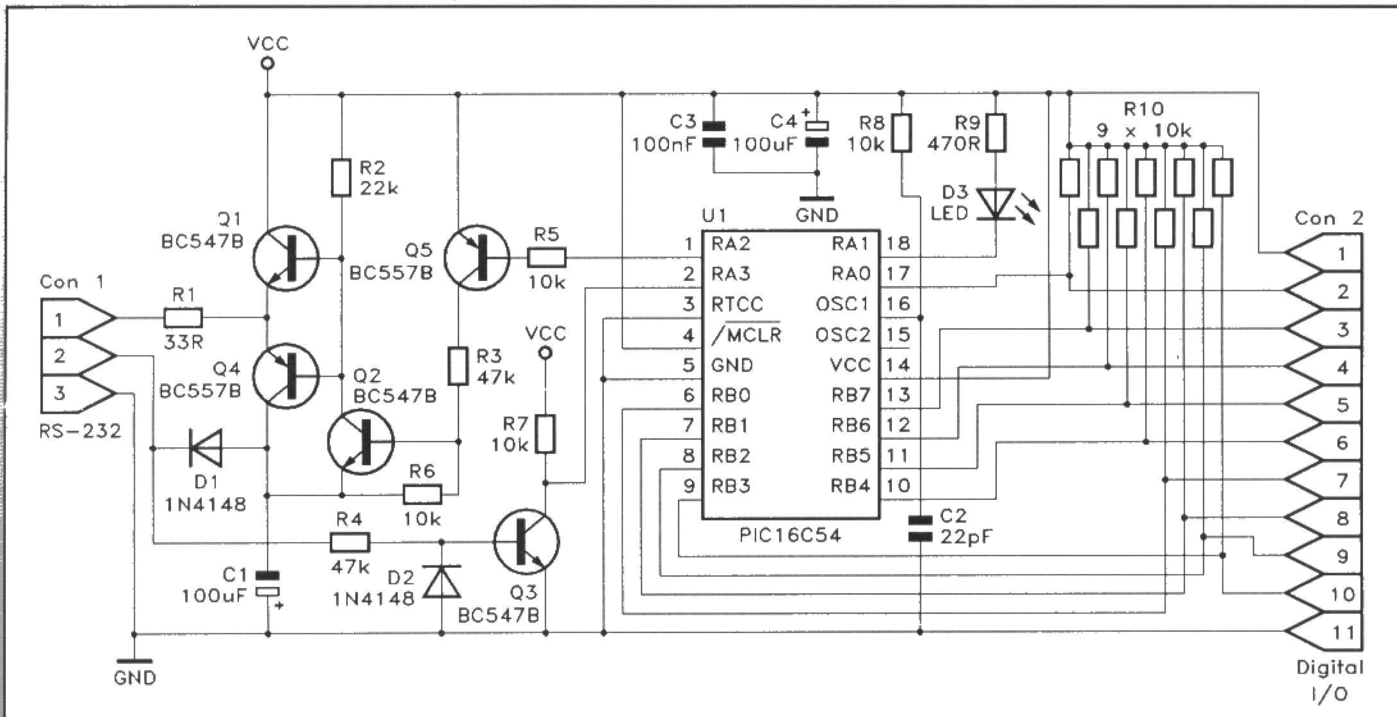


Figure 1. Circuit diagram.

The RM9011 is a single board, RS232 to 8-bit parallel input/output module, supplied ready-built with an extensive instruction leaflet and sample programs written in BASIC.

Figure 1 shows the circuit diagram of the module, which requires a single supply of +5V at an absolute maximum of 100mA. The voltage required for the RM9011 to transmit an RS232C logic 1 (−3V to −25V) is derived, ingeniously, from the host computer via D1 and C1. An 8-bit CMOS microcontroller is used to interface between the serial and parallel formats.

Setting Up

Figure 2 shows how to connect the module to any computer fitted with a standard 25-way, D-type RS232C port. No handshake signals are required, and the module sets its baud rate, bit format and parity on the first transmission from the host computer. Once this connection has been made, a simple program written in BASIC can be used for testing the system. Listing 1 shows such a program for PC-compatible machines. It should be fairly easy to modify this program to run on other computers. The program sets all bits as outputs and toggles them between logic 1 and logic 0 at short intervals. This allows each output to be checked with a logic probe, oscilloscope, multimeter or the test circuit, originally shown for the IBM PIO card project ('Electronics' Issue 43), which is reproduced in Figure 3. The suggested strip-board layout for the test circuit is shown in Figure 4. Photo 1 shows the test circuit fully assembled.

The period of the square-wave output may be adjusted by altering the number in line 160, presently set at 1000. A lower number will increase the frequency of the

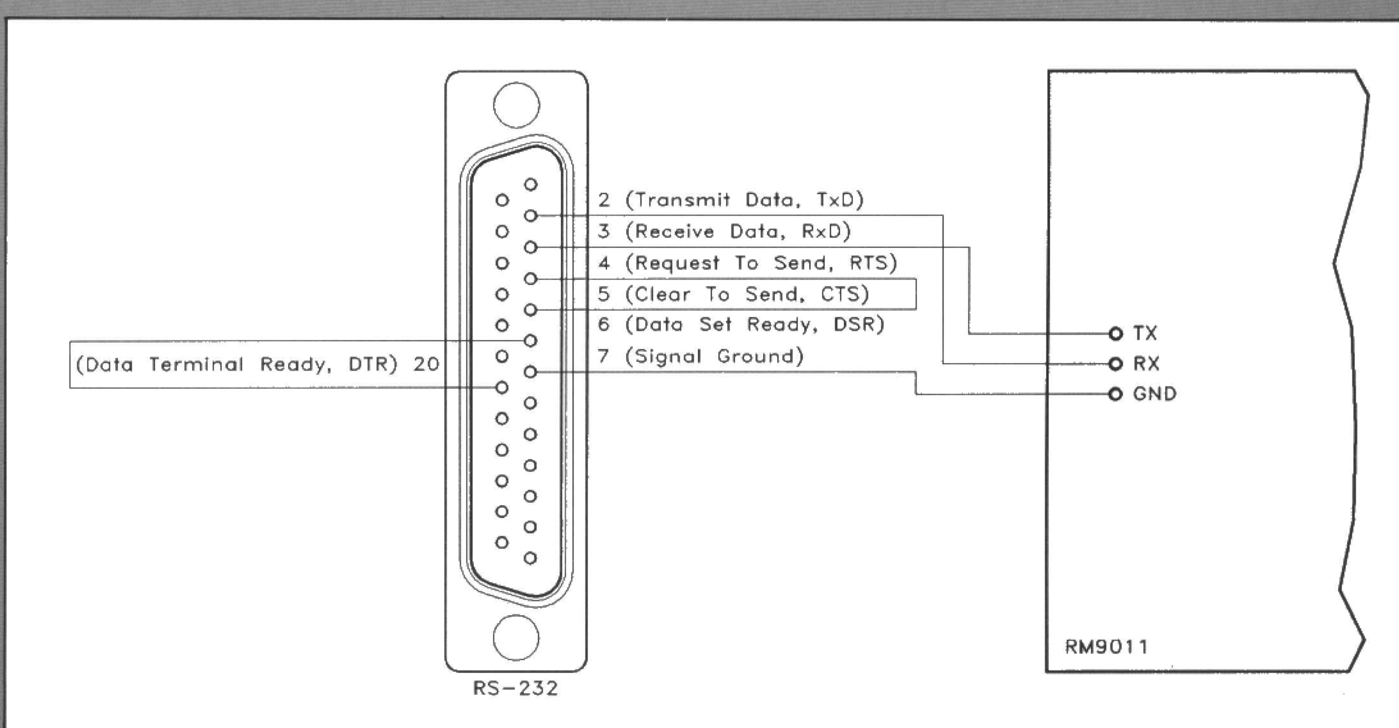


Figure 2. RS232 connections to the module.

```
10 OPEN "COM1:1200,N,8,1" AS #1  'Open file 1 as COM1,1200 baud,8 bits,no parity
20 PRINT #1,"!C0"               'Configure all lines as output
30 LINE INPUT #1,A$             'RM9011 answers
40 IF A$<>"!ACK" THEN 190              'If answer not !ACK then error
50 PRINT #1,"!W255"             'Set all lines high
60 PRINT "Logic 1"
70 LINE INPUT #1,A$             'RM9011 answers
80 IF A$<>"!ACK" THEN 190              'If answer not !ACK then error
90 GOSUB 160                    'Pause...
100 PRINT #1,"!W0"              'Set all lines low
110 PRINT "Logic 0"
120 LINE INPUT #1,A$                   'RM9011 answers
130 IF A$<>"!ACK" THEN 190             'If answer not !ACK then error
140 GOSUB 160                   'Pause...
150 GOTO 50
160 FOR F=1 TO 1000             'Delay subroutine
170 NEXT F
180 RETURN
190 PRINT "Error !"
200 END
```

Listing 1.

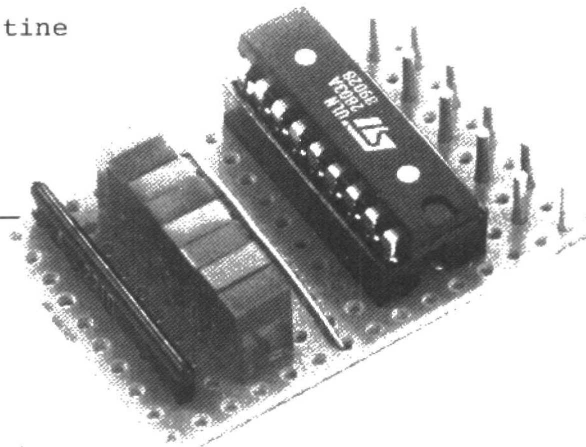


Photo 1. The suggested test circuit.

square-wave, and a higher number will have the opposite effect. When a logic probe is used to test D0 to D7 in turn, each will show logic 1 and logic 0 alternately, whilst an oscilloscope will show a slow square-wave. With a multimeter (set to its 5V DC (or higher) range), the display will show alternately 5V and 0V. When using the test circuit shown, the LEDs will flash on and off together.

Alternatively, one of the programs supplied with the module can be used for testing.

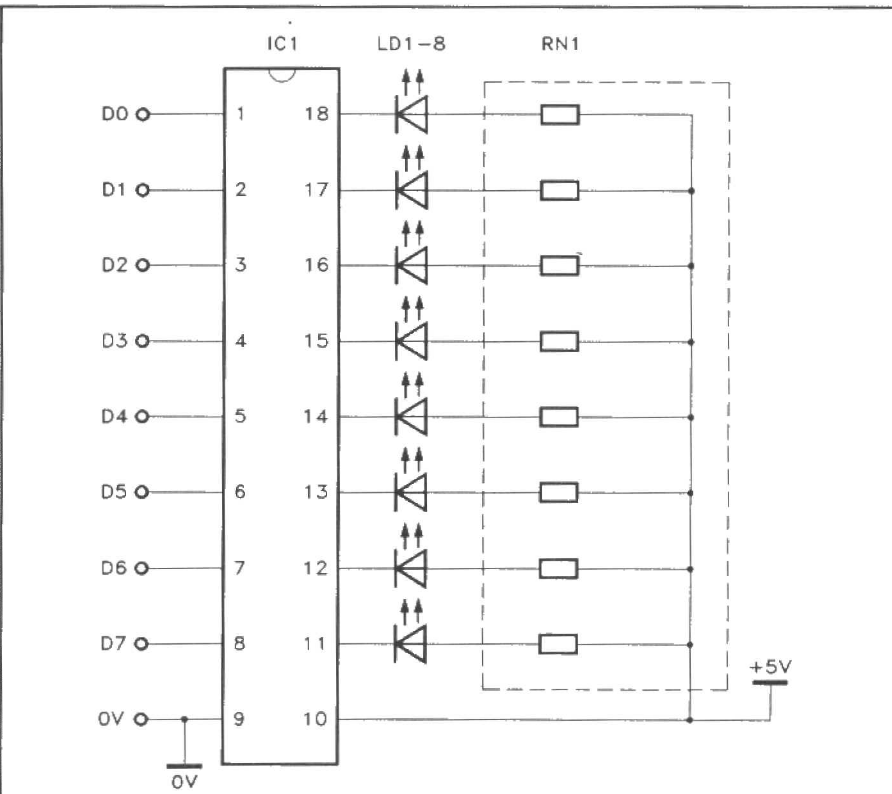
Control Commands

The RM9011 is controlled with standard ASCII characters sent from the host computer through the RS232 line. All commands start with an exclamation mark (!), and end with a carriage return (CR). The answers from the module have the same format.

The six different commands accepted by the module are:

!R (CR) Read byte
Read the inputs as a decimal byte value
Answer:
!Ixxx (CR), in which xxx = 3 characters from 000 to 255
If this command is executed on a line that is configured as an output, it will be read as low.

!Wxxx (CR) Write byte
Write the decimal byte value to the outputs, in which xxx is a 1 to 3 digit number ranging from 0 to 255
Answer:
!ACK (CR) if command accepted



IC1	ULN2803A	[QY79L]	1 off
LD1-8	Rectangular red LED	[YY45Y]	8 off
RN1	220R SIL resistor array	[RA24B]	1 off

Note: If separate +5V supply is used both RM9011 0V and supply 0V must be connected to CON2, pin 11.

Figure 3. Circuit diagram of a suitable test circuit.

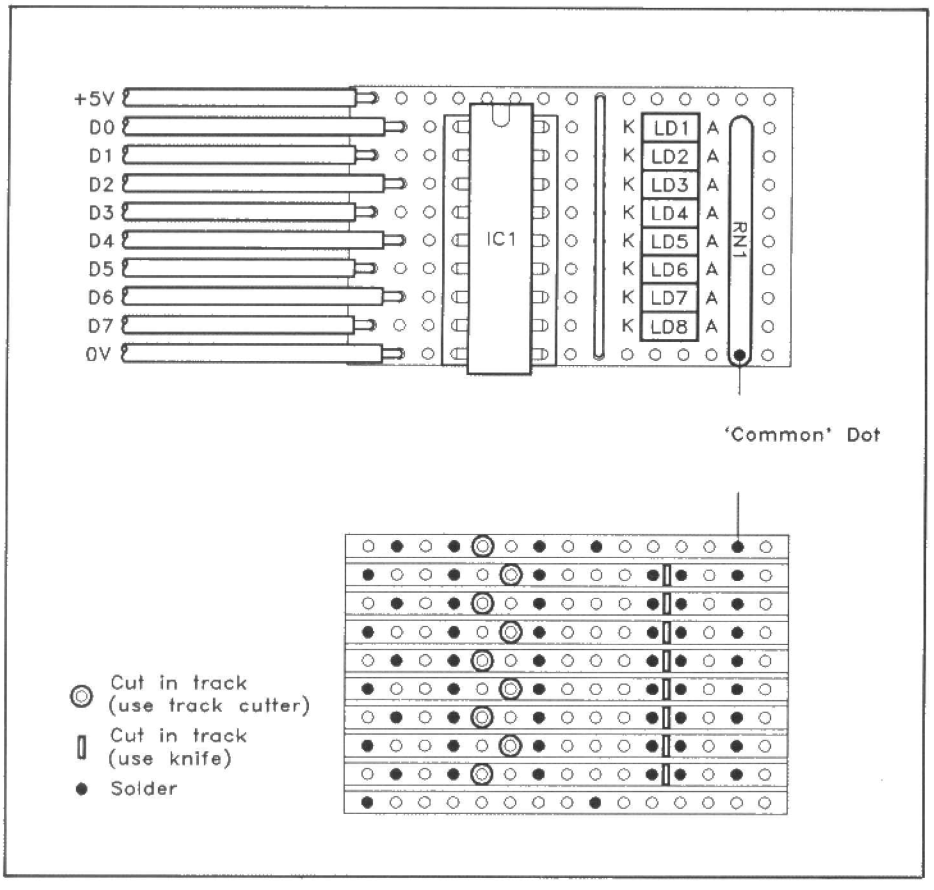


Figure 4. Suggested strip-board layout for the test circuit.

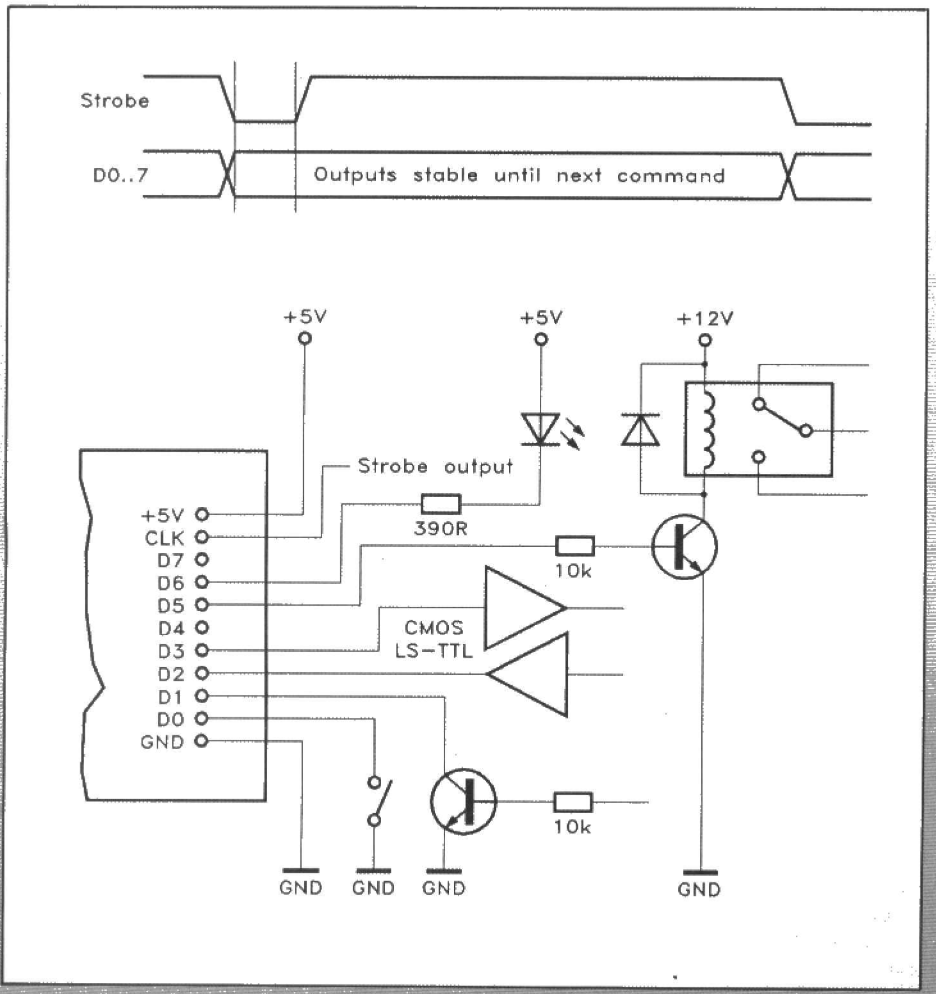


Figure 5. Example connections made to D0-D7.

!NACK (CR) if command invalid

!Cxxx (CR) Configure byte
Configure lines as input or output, in which xxx is a 1 to 3 digit number ranging from 0 to 255
Bit = 0 = Output
Bit = 1 = Input
Answer:
!ACK (CR) if command accepted
!NACK (CR) if command invalid

!RBx (CR) Read bit
Read input line x (0 to 7)
Answer:
!I0 (CR) if line low
!I1 (CR) if line high
If this command is executed on a line that is configured as output, it will be read as low.

!WBxy (CR) Write bit
Write y to output x, in which x is the output line (0 to 7) and y is the logic level (0=low, 1=high)
Answer:
!ACK (CR) if command accepted
!NACK (CR) if command invalid

!CBxy (CR) Configure bit
Configure line number x (0 to 7) as output (y = 0) or input (y = 1)
Answer:
!ACK (CR) if command accepted
!NACK (CR) if command invalid

The LED on the module (D3) briefly flashes each time a valid command is received from the computer.

Applications

The RM9011 finds many applications where a parallel to serial conversion (and vice versa) is required. However, note that as the module derives the negative voltage required for RS232 communication from pin 2 of CON1 (Rx), this pin MUST be connected to the host computer. Figure 5 shows some possible connections using the parallel I/O port.

One useful application for the module is in a computer-controlled security system. Several passive infra-red sensors (PIRs), positioned about the premises can be connected, through the RM9011, to a host computer, allowing an intruders movements to be mapped throughout the building.

Availability

The RS232 to 8-bit digital I/O converter module is obtainable from Maplin Electronics by mail-order or through their numerous regional stores The order code is LP85G and the price is just £16.95 inclusive of VAT.

INTRODUCTION TO Boolean Algebra

Part 1 by Graham Dixey C.Eng., M.I.E.E.

This is the first of three articles, written with the aim of providing an introduction to Boolean algebra that is both easy to follow, and useful for designing logic circuits that work. The intention is also to show that the word 'algebra' in the title need be no barrier to learning how to use it (after all, not everyone takes to mathematics naturally). In fact, learning the 'tricks' of Boolean algebra can actually be fun. Perhaps it will be possible to convince the sceptics of this; we'll try anyway!

Boolean or Switching Algebra?

When we call the algebra that we use for designing logic circuits Boolean algebra, we are actually acknowledging our debt to the 19th century mathematician whose name it bears, George Boole. It was he who propounded the original ideas. We could, and indeed sometimes do, call this algebra 'switching algebra', because the circuits designed using it can be classified as switching circuits. We even use our own notation for it, which is somewhat different from that employed by mathematicians.

Whatever we call it, the underlying ideas are concerned with TWO STATES only. These two states are opposites or, to use another term, they are 'complementary'. In general usage, we could be talking about complementary pairs such as YES and NO or TRUE and FALSE. However, we are specifically concerned with the idea of two states existing in electronic logic circuits. Therefore, we must choose two states that can be represented electrically. We must also ensure that we can tell them apart without any uncertainty. This is actually quite easy to do if we choose two quite different voltages, such as 0V and + 5V (the nominal values for one practical system). Next we shall need two symbols in order to have identifiable 'labels' for the two states. We choose '0' and '1' for these. This is no accident, since they are the digits of the binary number system, which we then have available for use in our logic.

Because this is a form of algebra, we adopt the usual algebraic convention and use the letters of the alphabet to stand for our 'variables'. In the algebra we learnt at school these variables could be anything: the cost of eggs, the number of objects of the same type in a group, and so on. In electronics there is less choice (sighs of relief!). The variables will simply be the inputs and outputs to/from a logic block, circuit or system. The algebra then becomes a generalised means of describing the logical relation between the inputs and outputs in such a logic arrangement.

For the present purpose, we are not concerned with the precise way in which the two logic levels, '0' and '1', are represented. While the TTL logic chip 'family' may use the values of 0V and +5V as the nominal levels of the two states, it is possible to have other logic types that use quite different voltages. This is unimportant as far as the algebra is concerned; it will still be valid no matter what the physical format. For example, the truth table for the OR gate in Figure 1 applies to ALL OR gates.

The Truth Table

This is possibly the most common and certainly the most easily understood method of representing the action of a switching circuit. Individual vertical columns are provided for each input and output. Normally, the first columns are reserved for the inputs, while the final column(s) is used to represent the output. Each column is given a heading (e.g. A, B, C, X, Y, Z) to identify each specific logic variable. Figure 1 shows how truth tables are typically laid out. There must be horizontal rows in the table for each possible combination of the input variables. The number of such combinations is equal to 2^n, where 'n' is the number of variables. Thus, where there are only two variables, there will be four combinations; where there are three variables, there will be eight combinations, and so on. As an example, for the OR gate of Figure 1, the combinations of the variables A and B are 00, 01, 10 and 11.

What does the truth table tell us? We can answer this by taking a look at one of those in Figure 1, for instance that of the AND gate. The first three lines (for the combinations 00, 01 and 10 of the variables A and B) all show that the output of the gate will be logic 0 under such conditions. Only when ALL input variables are equal to logic 1 will the output also be equal to logic 1. The last is true of all AND gates, regardless of the number of inputs present. Once we understand how one truth table works we can understand them all, since the idea is universal. It can be summed up as follows.

'The truth table shows which combinations of the input variables produce the logic 1 state at the output of the circuit. It then follows that all other input combinations result in a logic 0 output condition'.

It is reasonable to ask where the truth table comes from. It normally results from either of two situations. The truth table can be determined theoretically to describe the behaviour of a circuit yet to be designed, or it can be obtained by testing an existing circuit 'on the bench', noting the output states for all possible input combinations.

Algebraic Expressions

Let's start by looking at some of the simplest possible algebraic expressions:

(a) $F = A.B$ (The AND function: $F =$ A AND B)

(b) $F = A + B$ (The OR function: $F =$ A OR B)

(c) $F = \bar{A} + B$ (The NOT function: $F =$ complement of A)

Expressions (a) and (b) can be written for any number of variables A, B, C, D, etc, and the same rules apply in all cases.

Figure 2 shows the hardware used to implement these functions. I have used the US symbols and make no apology for

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

AND: $F=A.B$

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

OR: $F=A+B$

A	F
0	1
1	0

NOT: $F=\bar{A}$

Figure 1. Truth tables for the AND, OR and NOT functions.

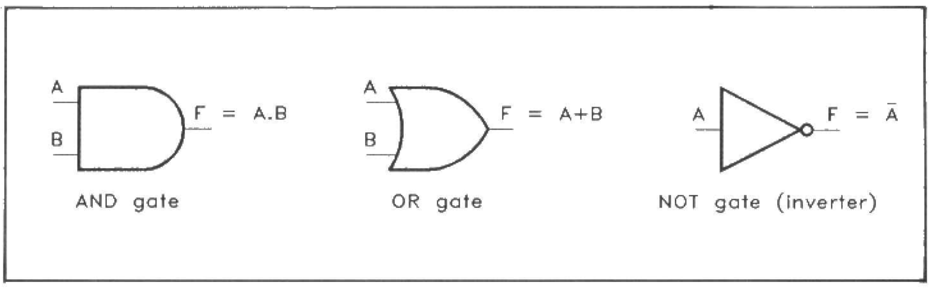


Figure 2. Circuit symbols for the AND, OR and NOT functions.

doing so, as they are in more common use than the equivalent BS symbols. The three equations above merely state in algebraic form, albeit more compactly, the same information as was previously contained in the truth tables. What they introduce are the three principal symbols used in the algebra. These are the dot (.) used for AND; the plus sign (+) used for OR and the bar ($\overline{\ }$) used for negation. Because the first two symbols have a more familiar context, newcomers to this subject often tend to say, 'A times B' and 'A plus B'. This is a temptation to be resisted. As far as negation is concerned, one may say 'NOT-A, the 'inverse' or 'complement' of A, or even A-bar.

It is possible to combine negation with either AND or OR to give, respectively, NOT AND (contracted to NAND) and NOT OR (contracted to NOR). The algebraic expressions look like this:

(d) $F = \overline{A.B}$ (F = A NAND B)
(e) $F = \overline{A + B}$ (F = A NOR B)

Naturally, it is possible to get very complex expressions that combine all the various forms but it is always possible to identify that, in the end, it all comes down to just AND, OR and NOT.

Exclusive-OR and Equivalence

There are two other functions of particular importance, having their own symbols. For two variables, A and B, they are:

(f) $F = A \oplus B$ [which is known as exclusive-OR (XOR)]
(g) $F = A \equiv B$ [which is known as equivalence (EQV), or exclusive-NOR (XNOR)]

The truth tables for these two functions are given in Figure 3 together with the circuit symbols and full algebraic expressions, that is:

XOR: $F = \bar{A}.B + A.\bar{B}$

This tells us that F = 1 when A = 1 or B = 1, but excludes the case when A and B are both 1. This can also be seen from the truth table (Figure 3), which should now be compared with that for the OR function (Figure 1).

EQV: $F = \bar{A}.\bar{B} + A.B$

The reason for naming this function 'equivalence' is obvious both from this equation and the truth table, shown in Figure 3. The output, F is 1 whenever both inputs have the same value (i.e. are equivalent), both being either logic 0 or logic 1.

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

XOR: $F=\bar{A}.B+A.\bar{B}$

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

EQV: $F=\bar{A}.\bar{B}+A.B$
(Also termed XNOR)

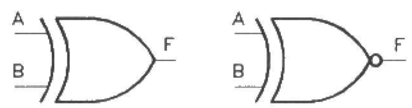


Figure 3. Truth tables and circuit symbols for the XOR and EQV functions.

Basic Axioms

There are a number of basic truths, or axioms, some of which will seem so obvious as to appear trivial. Some are extremely important, nonetheless. Look at each of the statements listed below and consider its truth as an exercise in simple logic. Help can be obtained by using the truth tables for the AND and OR functions given previously. As an example, consider the axiom:

$A + \bar{A} = 1$

If A = 1 then $\bar{A}$ = 0, or vice-versa. Either way round, the result is that we are always ORing 1 with 0, which occupies the second and third lines of the OR truth table. In both cases, the value of F is 1, thus proving this basic axiom.

$0 + 0 = 0$	$0.0 = 0$
$0 + 1 = 1$	$0.1 = 0$
$1 + 1 = 1$	$1.1 = 1$
$A + 0 = A$	$A.0 = 0$
$A + 1 = 1$	$A.1 = A$
$A + A = A$	$A.A = A$
$A + \bar{A} = 1$	$A.\bar{A} = 0$

Basic Laws

There are also a few basic (and self-evident) laws as follows:

(i) A.B = B.A; A + B = B + A [commutative law]
(ii) A + B + C = (A + B) + C = A + (B + C) = (A + C) + B
(iii) A.B.C = (A.B).C = (A.C).B = A.(B.C) [associative laws]
(iv) A + (B.C...) = (A + B).(A + C).(A + ...
(v) A.(B + C + ...) = A.B + A.C + A... [distributive laws]

The commutative law tell us that the order of the variables is not important. The associative law tells us that, within an AND or OR expression, variables may be associated by brackets without affecting the value of the expression. The distributive law operates on brackets in a similar way to conventional algebra, allowing an expression to be expanded by 'multiplying out'.

De Morgan's Laws

These laws are important enough to be allowed a paragraph of their own. They are quite simple and will be found useful in many situations. For two variables they can be expressed in two ways. The form for more than two variables follows easily from the basic form.

(vi) $\overline{A + B} = \bar{A}.\bar{B}$
(vii) $\overline{A.B} = \bar{A} + \bar{B}$

Notice that the left-hand side is a NOR expression for law (vi), and a NAND expression for law (vii). Later on, this will be seen to be useful when designing logic circuits using NOR or NAND logic. However, the de Morgan's relations are also very useful in the process that we call simplification or 'minimisation', very often an essential part of logic circuit design.

The Negation Bar – a Word of Warning!

There is a point worth mentioning now, since it often trips up the unwary beginner. The negation bar over a variable or expression is rather like the minus sign used for negative quantities in arithmetic. In fact, we can use it in a similar way. Thus, in the case where we have (− −) in arithmetic, we know that the two minuses give us a plus. Similarly, in Boolean algebra, two bars OF THE SAME LENGTH over a variable or term cancel out. Note the emphasis on the phrase 'of the same length'. This is the trap for the unwary. Consider the following example:

If $F = \overline{\overline{A.B}}$ then F = A.B (since the negation bars are the same length).

Now consider these two examples:

(a) $F = \overline{\bar{A}.B}$

and

(b) $F = \overline{\bar{A}.\bar{B}}$

The bars do not cancel out in either of these two expressions. In the first case, (a), one bar negates the variable A only while the other, longer, bar negates the whole term. What this expression really means is 'the NAND of NOT-A and B', which is quite different from the 'A AND B' that we should have ended up with had we cancelled out the two bars.

Taking the second case now, each variable has its own bar and the whole expression is then negated. Again we cannot cancel out the bars. It obviously (?) means 'the NAND of NOT-A and NOT-B'. Bear this point in mind when examining complex expressions where there may be a number of bars of varying lengths.

Boolean Expression

There are two identifiable forms of Boolean algebraic expression. One of

these is known as the 'sum of products' form, and a typical example might be as follows:

$F = A.B.C + A.\bar{B}.C + \bar{A}.\bar{B}.C$

It is easy to see why this is so called; it looks like the addition of a number of products, though strictly speaking it isn't, of course. This is just a convenient title to differentiate it from the other form which is known as the 'product of sums' form. An example of this is as follows:

$F = (A + B + C).(\bar{A} + B + C).(A + \bar{B} + \bar{C})$

Again, the reason for calling it by this name is obvious.

To make a further distinction, consider a second example of the sum of products form:

$F = A.B + B.C + \bar{A}.C$

What distinguishes this from the first example of this form? The answer is that, whereas both expressions contain the variables A, B and C, only in the first example does EVERY term contain ALL three variables. In the second case each of the three terms contains only two of the three variables. There are many such examples. The first type of expression is said to be in CANONICAL form; the second type is said to be NON-CANONICAL. Another example of a non-canonical expression is $F = A + B.C$. Again there are three variables, but two (B and C) are missing from the first term and one (A) is missing from the second term. The reason for introducing these apparently unwieldy terms is that simplification of an algebraic expression often involves converting it from canonical to non-canonical form, much easier than it may sound! Conversely, it is sometimes useful to be able to perform the opposite conversion, from non-canonical to canonical form, which involves a simple trick.

The use of the term 'trick' is not inappropriate here. There are many very straightforward procedures in Boolean algebra that are quite easy to pick up and which can be used to design digital circuits that work. However, as in other avenues of life it is possible to be that little bit cleverer and produce an alternative circuit that performs exactly the same function as an original design but uses less gates, consumes less power, involves simpler circuit board construction and so on. Thus, as in analogue design, there is rarely a unique solution to a problem, merely the range of possibilities that reflect various designers' individual approaches and techniques. I shall try to illustrate some ideas as we proceed.

Minterms and Maxterms

Let's go back to a canonical sum of products expression, a nice easy one:

$F = \bar{A}.\bar{B} + A.B$ (the EQV function you will remember)

This consists of two terms featuring the variables A and B. Each term in this type of expression is called a MINTERM because it represents just one line of a truth table. For example, the first term above stands for the line $A = 0$ and $B = 0$; the second term stands for the line where $A = 1$ and $B = 1$. That's simple enough, isn't it?

Now consider a product of sums expression, again in just two variables:

$F = (\bar{A} + \bar{B}).(A + B)$

Each of these bracketed terms is known as a MAXTERM because it represents ALL lines of a truth table BAR ONE. Now this is not so obvious, so we shall have to work a bit harder to show the truth of this statement. It helps in this case that we know what all the lines of the truth table are: $\bar{A}.\bar{B}$, $\bar{A}.B$, $A.\bar{B}$ and $A.B$. Now consider the first bracketed term, namely $(A + B)$. The meaning of this term is that it represents all those lines for which either $A = 0$ or $B = 0$. If the statement above is true there should be THREE lines that follow from this, since the truth table has four lines altogether. Consider the four lines of the truth table:

00; 01; 10; 11

For how many of these terms is either A or B equal to 0? The answer is quite clearly THREE, in fact the first three since, in the fourth term A and B are both 1. Try it now for the second bracketed term. For how many terms of the possible set of four is either A or B equal to 1? The answer is now the last three. This will always be true, no matter how many variables are involved. For example, the maxterm $(A + B + C + D)$ represents fifteen of the sixteen possible lines of the truth table.

Why not try it and see?

Simplification of Switching Functions

In general, the simpler the algebraic expression that describes a particular switching circuit, the simpler and cheaper will be the hardware requirements. Thus, when we are faced with an algebraic expression for a particular requirement, we should always consider how we can make the expression as simple as possible. It is quite surprising how many a complex expression reduces to something very simple indeed. This point will be illustrated graphically soon. The process of simplifying an algebraic expression is often referred to as 'minimisation'. There are several techniques for minimising an expression. One way of doing so is to make use of the various axioms and laws that we met earlier. This method is based upon the ability to recognise when a particular situation calls for a particular law to be applied. Some of the techniques become quite convoluted. Ability in this matter depends upon intellect and experience. The more one attempts the more one learns.

One basic law that is especially useful is the one that says:

$A + \bar{A} = 1$

The terms of a sum of products expression (the form in which most Boolean expressions naturally occur) are examined to see if they can be factorised to yield an OR expression of the type above. Whenever such a term is found it can be replaced by unity, thus resulting in a simplification. The process may well have to be repeated over several lines if the original expression is complex. We shall look at an example of this type now, but just before doing so, it is necessary to point out one feature of this method that might not be obvious otherwise. This is that, in order to carry out the factorisations, it is possible to use any term any number of times, if this helps. This will be obvious from the following:

EXAMPLE. Simplify $F = \bar{A}.\bar{B}.C + \bar{A}.B.\bar{C} + \bar{A}.B.C + A.\bar{B}.C + A.B.C$

If we examine this, we see that the first and third terms contain a common factor [$\bar{A}.C$, giving $(\bar{B} + B)$]; the second and third terms also contain a common factor [$\bar{A}.B$, giving $(\bar{C} + C)$]; the fourth and fifth terms contain the common factor $A.C$ [giving $(\bar{B} + B)$]. After this factorisation the expression looks like this:

$F = \bar{A}.C(\bar{B} + B) + \bar{A}.B(\bar{C} + C) + A.C(\bar{B} + B)$,
From which $F = \bar{A}.C + \bar{A}.B + A.C$ [since all bracketed terms $= 1$]

We can factorise further because the first and third terms contain the common factor C. So we get:

$F = C(\bar{A} + A) + \bar{A}.B$,
$= C + \bar{A}.B$

This repeated use of a basic law is a common algebraic technique for simplifying expressions. However, when there are a large number of terms it becomes rather unwieldy to handle in this 'longhand' manner. But there is a technique that is based on exactly the same procedure but is automated for greater convenience. It is called the Karnaugh map and we shall meet it in the second of these articles. For now we shall continue with some more pure algebraic processes.

Using De Morgan's Theorem

The importance of this theorem cannot be undervalued. It crops up again and again. It is useful, for example, for converting an expression from one form to another. The simplification carried out above commenced with the expression in the sum of products form. This is usually the more convenient way. However, if the original expression is of the alternative form, i.e. the product of sums, all is not lost; we can use de Morgan's theorem to turn it into sum of products form. Until one is fully familiar with this theorem, it is quite useful to have a method for applying it that consists of a series of well-defined steps. They can be stated as follows:

(a) Replace the 'dots' between the terms with 'pluses'
(b) Invert each term
(c) Invert the whole expression.

The same procedure can be used for converting from sum of products notation, to the product of sums form if, in line (a)

we reverse the symbols being replaced i.e. replace the 'pluses' with 'dots'. To make this clearer, let's take a very simple example to start with:

EXAMPLE 1. Use de Morgan's theorem to change the form of the expression F = P.Q. We will do this in three steps (as stated above), noting the result of each step as we go. (N.B. when we are used to the idea we carry out all three steps in a single line. For now we shall 'walk before we try to run'!)

(a) $P + Q$ [exchanging the dot for a plus]
(b) $\bar{P} + \bar{Q}$ [inverting each term]
(c) $\overline{\bar{P} + \bar{Q}}$ [inverting the whole expression]

Thus we end up with the expression, $F = \overline{\bar{P} + \bar{Q}}$. Note that we could equally well say that $\bar{F} = \bar{P} + \bar{Q}$, since it doesn't matter which side the negation bar goes on.

There was a good reason for using P and Q here instead of the more usual A and B. It is essential to get hold of the idea that de Morgan's theorem can be applied in exactly the same way whether the expression ACTUALLY consists of just two terms (whatever they are called), as in the example just taken, or whether P and Q each really represent a more complex arrangement of variables. To take another example to illustrate this:

EXAMPLE 2. Use de Morgan's theorem to convert the following expression to the alternative sum of products form.

$F = (\bar{A} + B).(A + B)$

This expression is in exactly the same form as the previous one; the difference is that P is represented by the term $(\bar{A} + B)$, while Q is represented by the term $(A + B)$. We have to force ourselves to ignore the contents of the brackets at this stage and merely regard each bracketed term as if it were a simple variable. Let's perform the same series of operations on this expression and afterwards compare the result with that obtained in the first example.

(a) $(\bar{A} + \bar{B}) + (\bar{A} + B)$ [exchanging the dot for a plus]
(b) $\overline{(\bar{A} + \bar{B})} + \overline{(\bar{A} + B)}$ [inverting each term]
(c) $\overline{\overline{(\bar{A} + \bar{B})} + \overline{(\bar{A} + B)}}$ [inverting the whole expression]

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

$$F = \bar{A}.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + \bar{A}.B.C + A.\bar{B}.\bar{C} + A.B.\bar{C}$$

Figure 4. Obtaining an algebraic expression from a truth table.

Thus $F = \overline{(\bar{A} + \bar{B})} + \overline{(\bar{A} + B)}$,
or $\bar{F} = (\bar{A} + \bar{B}) + (\bar{A} + B)$.

Doesn't this seem to be of the same form as the result of Example 1? All we need to do is regard the bracketed terms as being represented by P and Q as explained previously.

With the more complex expression of Example 2, we don't stop at this point since it is not yet in sum of products form. We have to apply de Morgan's theorem again. This time we apply it to the bracketed terms themselves. Since there are two bracketed terms we shall carry out the same procedure twice, once for each term. For the term $\bar{A} + \bar{B}$, we shall get, first (a) $\bar{\bar{A}}.\bar{\bar{B}}$; then (b) $\overline{A.B}$; and finally (c) A.B. Similarly, the second term $\overline{A + B}$ will give us $\bar{A}.\bar{B}$. All we have to do now is to put these new expressions back into the first result obtained, so that finally:

$F = A.B + \bar{A}.\bar{B}$

This is of the required sum of products form.

Obtaining an Algebraic Expression from a Truth Table

We have seen that the truth table and the Boolean expression are alternative forms of the same thing. The truth table lets us see quite clearly which input combinations produce a logic 1 output. The algebraic expression is useful because it gives us something to manipulate (as when we simplify, or just change its form) so as to design a circuit to optimise, for example, the hardware or power requirements. If we have a truth table it is quite an easy matter to extract the corresponding algebraic expression from it. The only snag is that such an expression will rarely be the simplest it can be (known as a 'minimal' expression). However, we can then apply our techniques to minimising it once we have it.

Figure 4 shows a truth table for a three-variable logic circuit with inputs A, B and C. The output F is at logic 1 for five of the eight possible input combinations. In other words, there are five possibilities, each yielding the condition F = 1; this itself implies the use of the word OR! In general, we are saying (upon examination of the truth table) that F = 1 when we have input combination 1 (i.e. the first line that results in F = 1) OR when we have input combination 2 (the next one that gives F = 1) OR when we have input combination 3 (meaning the next one...) and so on. This can be stated in the algebraic form (far superior to the wordy version above!) by writing the possibilities out as an OR function of all the lines for which F = 1. This will be in the sum of products form of course. For the truth table of Figure 4 we shall then have:

$F = \bar{A}.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + \bar{A}.B.C + A.\bar{B}.\bar{C} + A.B.\bar{C}$

This can certainly be simplified. We have already seen an algebraic technique for doing so. In the next article we shall look at the use of the Karnaugh map, a much more convenient and very powerful way of simplifying expressions of this type.

Tuning into Capital

by Alan Simpson

The Number One Station – for the Number One Capital!

Capital Radio has several claims to fame. Established in 1973, it was Britain's first legal commercial radio station — and the first licensed station to provide London with popular music 24 hours a day. With a revenue of £37 million, and some 5·7 million listeners clocking up over 50 million listening hours every week on its two services, the station is not only the largest in local UK radio, but also one of the world's largest commercial radio stations.

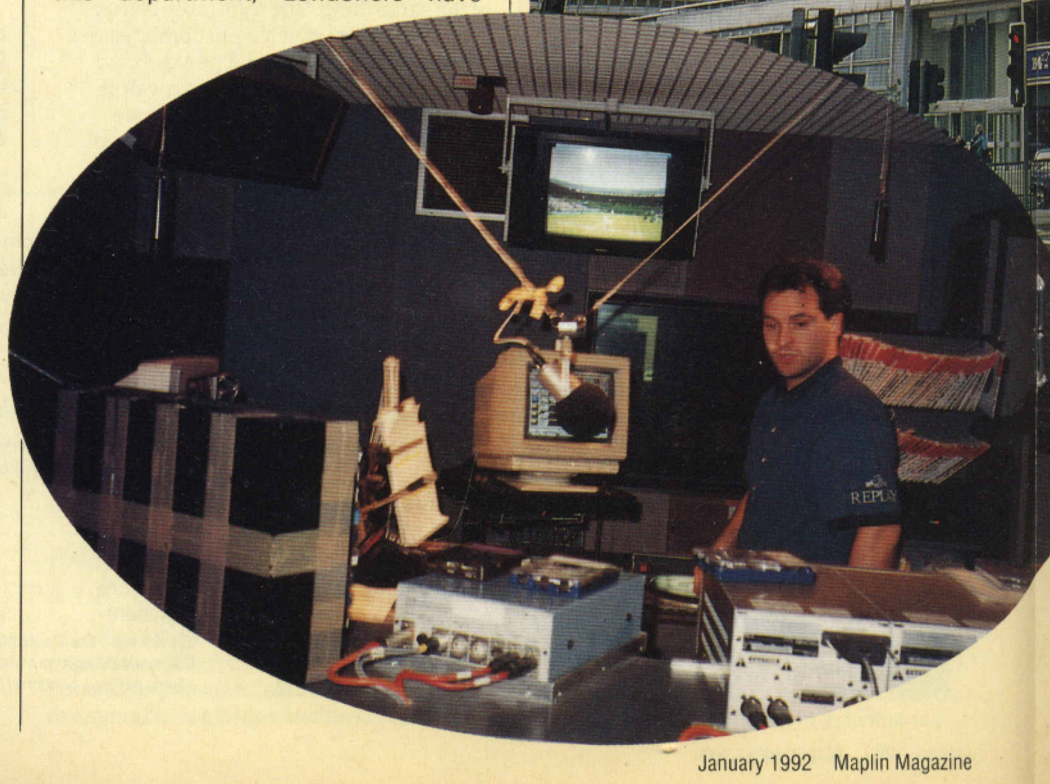
Today, London has two separate Capital radio stations — the well-established Capital FM, and the more recent Capital Gold which broadcasts classic hit records from the last three decades. If it is Madonna you crave, then tune into 95·8MHz FM. If you want to hear the Beatles, Stevie Wonder or the Stones, then head the dial towards 1548KHz AM. The station's audience divides almost as clearly as the music. The FM service attracts the under-35 year olds while the station devoted to 'golden oldies' beams in to the 35+ group. Even so, Capital is not short of competition; rivals include the BBC's well-established Radio One and Greater London Radio services together with such 'newcomers' as Jazz FM, Melody Radio, Kiss FM, the expanding number of local community stations and the few 'pirates' remaining after the Government clamp-downs had done their worst.

Music Mayhem

Despite the competition, Capital simply has no equal when it comes to popular music. The two independent channels belt out music 24 hours a day, every day. When not transmitting the 'tops of the pops', the stations are organising Music Festivals, London Blues Festivals, and Radio Jazz Parades. If there is a top event in London, the chances are that Capital has been involved in some way. Helping to keep the music on the road is the Capital Radio 'Rig', a massive 45-foot long outside broadcast vehicle which, in the station's words, resembles a 'giant ghetto blaster on wheels'. With a fully equipped control room, DJ console, video wall and remote-controlled stage, the Rig is used at a variety of outside broadcasts. Along with the news team's Renault Espace van, the Rig is fitted with 'link' equipment comprised of a relatively low-powered radio transmitter and a directional aerial mounted on a retractable telescopic mast. Such apparatus enables signals to be sent back to one of a number of receiving sites, and then back to the Capital Tower studios via a special BT digital (PCM) music line.

Not Just a Music Station

However, Capital Radio doesn't just provide music. The station's Community Affairs division has been in operation since 1976, three years after the station was first launched. 'Helpline', the station's off-air information, advice and referral service, has taken an incredible 2000,000+ calls since then. The Helpline team deal with problems which range from a query about the 1934 FA Cup winner, to more intimate personal queries. By phoning this department, Londoners have



OUT AND ABOUT

access to vital information on virtually any subject that affects their day-to-day lives. This is undoubtedly useful for those who live in one of the world's largest and busiest cities, although it is debatable whether relaying up-to-the-moment information on roadworks in Croydon, or a gig in Woolwich, will be of much interest to the listener resident in Golders Green (North West London)! The Capital Flatshare Service helps to find accommodation for up to 1,000 people every month while the Capital Jobfinder Desk, situated in the Capital foyer, specialises in finding jobs for the under 25s (on Capital FM) and the over 25s (on Capital Gold). This computerised service not only keeps tabs on the jobs that are available, but also advises on training, retraining, job-sharing and childcare options. Capital also assists a great many charities and community groups which are seeking assistance in finding volunteers or equipment. With such a range of services, in addition to various other educational, careers, health and fitness projects which take place throughout the year, Capital can be rightfully proud of its Community Affairs activities.

A Good Sport

Each Saturday in the season, Capital Gold Sport covers some 9 or 10 football matches, relying on direct, permanently set-up music circuit telephone links from London's many football stadiums. (Outside of London however, Capital make use of temporary 'booked' circuits). Currently, Capital is setting a pioneering pace by replacing the existing analogue circuits with new BT ISDN–2 digital telephone lines. As Peter Jackson, Capital Radio's chief engineer, explains: "We are typically installing a circuit, with a 10kHz bandwidth, from the grounds to Capital Tower. Such two-way ISDN circuits (which allow a narrow-bandwidth 'talkback' facility) do not come cheap, can only be used in locations with access to a System X exchange, and in addition the circuit rental fees are high." However, Peter still believes that ISDN is a great idea: "There is no reason why we shouldn't simultaneously use two ISDN channel lines to facilitate stereo transmissions. It is, unfortunately, a lot more difficult to compress audio than video."(In the latter, redundancy in the field of each picture provides considerable scope for compression.)

The Route to the Transmitters

The output of on-air studios is sent by music circuits to transmitters. These high-grade circuits connect the Euston Centre studios to the NTL-operated transmitters at South Norwood (FM) and Saffron Green (AM). The 4kW (ERP) VHF transmitter used by the FM service is also equipped with an RDS Radio Data System) encoder which can provide a display of the station name on a suitably equipped receiver, as well as several other more useful functions (For example, a suitably equipped car radio will switch automatically to the nearest station providing a traffic report – which for most of London will be Capital) Meanwhile, the AM channel makes use of a 100kW (ERP) medium-wave transmitter. No wonder you can pick up the station in Northern France! In common with an increasing

Above: 'Capital Tower', the Capital Radio studio complex near Euston Station.
Left and right: Two of the studios used for programme presentation.

Below: The Flying Eye team; from left to right, Pam Spriggs, Russ Kane, and Hazel Murray.

number of companies, Capital relies on BT lines into the offices – and those provided by Mercury for cheaper outward calls. The station has 140 inward telephone lines which, at certain peak 'phone-in' times, could all be busy. Meanwhile, the 30 Mercury lines are routed directly to the local Mercury exchange. The station, also has direct lines to the Meteorological Office (the 'Met') and various transport offices. "We have a hefty communications investment" says Peter.

The computer investment is similarly high. Each studio has its own terminal, linked to a Local Area Network (LAN) which displays road traffic and weather information. Programme playlist compilation is handled by yet another computer, this time running a specially designed program (originating from the United States) known as 'Selector'. The three-strong computer team has written its own scheduling program for commercials which runs on the inhouse LAN.

"Commercial Radio, like that of commercial TV, is all about selling to audiences, and a major investment in software can be easily justified", says Peter. At the same time, the records must be listed in playing order so that 'needle-time' fees can be paid to the appropriate artistes and record companies. Even if only half a track is played, an appropriate fee has to be paid. "Life has become much easier (and much speedier) since we computerised this activity" states Peter.

Sticky Fingers

A specially ventilated library holds all the music. These days, most of the music is held on CDs – even Capital Gold relies on the 'Best of' CD format. Before playing, the CDs are loaded into a cartridge which helps to avoid any problems with the programme presenters' sticky fingers. The CD system is very popular among broadcasters because of its many advantages. CDs have a longer life than records; before CD, radio stations would get through several copies of a single — simply because the lead-in groove, used for 'cueing up', would always wear out before the rest of the record, and any scratches caused by usual DJ wear and tear would eventually render it 'unbroadcastable'. In addition, a CD offers better sound quality than a vinyl record (on the radio at least!), the smaller size of the disc is welcomed by the record librarians – and at last there is a sound carrier which even the clumsiest DJ would find hard to damage! In addition, a CD is also far simpler than a record to cue effectively. The DJs do not have sole choice of the music they play. It is mostly chosen in association with their producers and is scheduled in order to ensure that no record is overplayed, or come to that, neglected.

Capital Radio has a total of nine studios at its Euston complex (near the famous railway terminus). Three of these are self-operated (on-air) studios, each of which is equipped with a mixing console, this accepting the various different programme sources. Other studio equipment normally includes two CD players, two turntables, six or more cartridge players (for jingles and adverts) three or four microphones, and a pair of loudspeakers for monitoring the outgoing programme (these are automatically muted when a microphone fader is turned up, to eliminate the possibility of unwanted feedback). Five of the other studios are used for production work, which includes News and Talks output, interviews, special features, commercials and programme trailer production.

The ninth studio is used to record and mix down live music. This large studio can accommodate up to 20 musicians and is equipped with an SSL 24-track mixing console with 32 input channels. There is an Otari MTR90 24-track recorder, with additional Studer A80 and A810 ¼inch stereo machines to record the final mix. This studio also features video playback facilities.

Power from the People

It takes a staff of nearly two hundred to keep the station on the air 24 hours a day, seven days a week. 40 of these are DJs, and include Chris Tarrant, presenter of the FM breakfast show, and Tony Blackburn, who left Greater London Radio to join Capital Gold. Almost in the same league of fame is 'Commander' Russ Kane who broadcasts from Capital Radio's Flying Eye, Britains first ever traffic-spotting plane. Based around a twin-engined Piper Seneca, this flies low over London (weather permitting) and provides both FM and Gold listeners with up-to-the-minute traffic news.

Capital Radio has been a hit with London since it first went on the air at 5am on October 16th, 1973. It could now become a hit for seven lucky 'Electronics' readers who enter the competition below.

Competition

Here's your chance to visit the Capital Radio studios in London and find out at first hand what makes London's top radio station tick. A tour for two, conducted by Capital's Chief Engineer, Peter Jackson, is the top prize in this month's competition. Six Capital Radio T-Shirts are on offer as runner-up prizes. The catch? All you have to do is to answer the following questions and be the first all-correct name to be drawn out of our new editor's (newish) hat. Send your entries (please don't forget your name, address and 'phone number) to: 'Capital Radio Contest', The Editor, Electronics – The Maplin Magazine, P.O. Box 3, Rayleigh Essex, SS6 8LR.

Speed is of the essence. The contest closes January 31st 1992 – and the best of luck! Please note that employees of Maplin Electronics and members of their families are not eligible to enter. In addition, multiple entries will be eliminated from the draw.

1. Capital FM is the world's most popular commercial music station. What does FM stand for?
a) Friendly Music
b) First Memory
c) Frequency Modulation
d) Frequency Medium

2. What does Capital Gold signify?
a) The Golden Age
b) The station of Golden Oldies
c) Floating Gold Fish
d) Loadsa Money

3. Who is unlikely to be top of the Capital pops?
a) Kim Basinger
b) Sinead O'Connor
c) The Beach Boys
d) Vanilla Ice

4. Spot the odd one out
a) Dave Cash
b) Kenny Everett
c) Jimmy Savile
d) Ken Livingstone

PART FIVE
The Resistor-Inductor-Capacitor Circuit
by Philip Lawton

PREDICTING WAVESHAPES USING A COMPUTER

Introduction

In Part 4 of this series, the inductor was introduced into the circuit configuration under examination. In this part, a capacitor is also introduced making the Resistor-Inductor-Capacitor configuration, and we will explain how to predict some of the transient and steady state waveshapes that appear in this circuit.

The Resistor-Inductor-Capacitor (RLC) series circuit, as shown in Figure 15, is used to illustrate how to apply the fundamental laws in order to obtain two very useful 'rate' equations. This explanation is followed by a description of a computer program used to evaluate the 'rate' equations for any applied input emf, and to plot the predicted waveshapes. As before, two program listings are given for both IBM PC GW–BASIC, and BBC Acorn BASIC. Adapting the programs for other machines may be possible by just altering the statements which plot the display on screen.

The input is chosen as a constant of 1 volt, and a sine wave at a frequency equal to the natural frequency of the RLC circuit. The predicted current and potential difference of the capacitor illustrates a transient followed by a steady state. The steady-state sinusoid has a magnitude which is *greater* than the magnitude of the applied sinusoid.

Finally, the predictions are related to the phasor diagram. 'Things to do' are also suggested.

Fundamental Laws

The simplest laws are always the best. A useful law for the capacitor relates the current (i) to the product of the capacitance (C), and the rate of change with respect to time of potential difference of the capacitor (sv). The law is:

i = C (dv/dt)
(derived from q = C.v)

This law predicts the fact that when a current exists then the potential difference of the capacitor will change.

A useful law for the inductor relates the induced emf (emf) to the product of the inductance (L), and the rate of change with respect to time of the current (si). The law is:

emf = L (di/dt)
which is derived from:
emf = N (d0/dt)
and
L = N (d0/di)

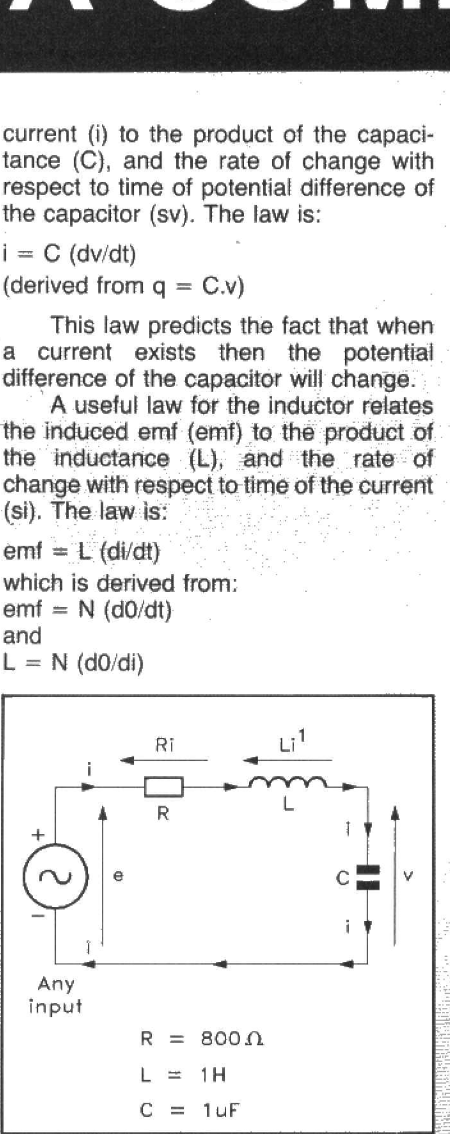


Figure 15. The Resistor-Inductor-Capacitor series circuit.

This law predicts the fact that when a rate of change of current (magnetic flux) exists, then an emf is induced in the coil of the inductor.

Equations

Equations for modelling the RLC circuit can be derived using the above laws, Kirchhoff's voltage law, and Ohm's law. Note that the waveshape of the applied input signal is represented by the symbol e (volts), and that the results are a current i (amps), and a capacitor potential difference v (volts). These equations are:

1) e = (R.i) + (L.(di/dt)) + v
2) i = C (dv/dt)

where:

- e is the value of the applied emf,
- R is the value of the resistor,
- i is the value of the current (in amps),
- L is the value of the inductor,
- v is the value of capacitor potential (volts),
- C is the value of the capacitor,

Equations to predict the rate of change of inductor current with respect to time (si), and the rate of change of capacitor potential with respect to time (sv), can be obtained by rearranging equations (1) and (2) to yield:

1.1) di/dt = (–R/(L.i)) – (1/(L.v)) + (1/(L.e))
2.1) dv/dt = 1/(C.i)

These equations can be used to evaluate the rate of change with respect to time of the inductor current (di/dt), and the rate of change with respect to time of

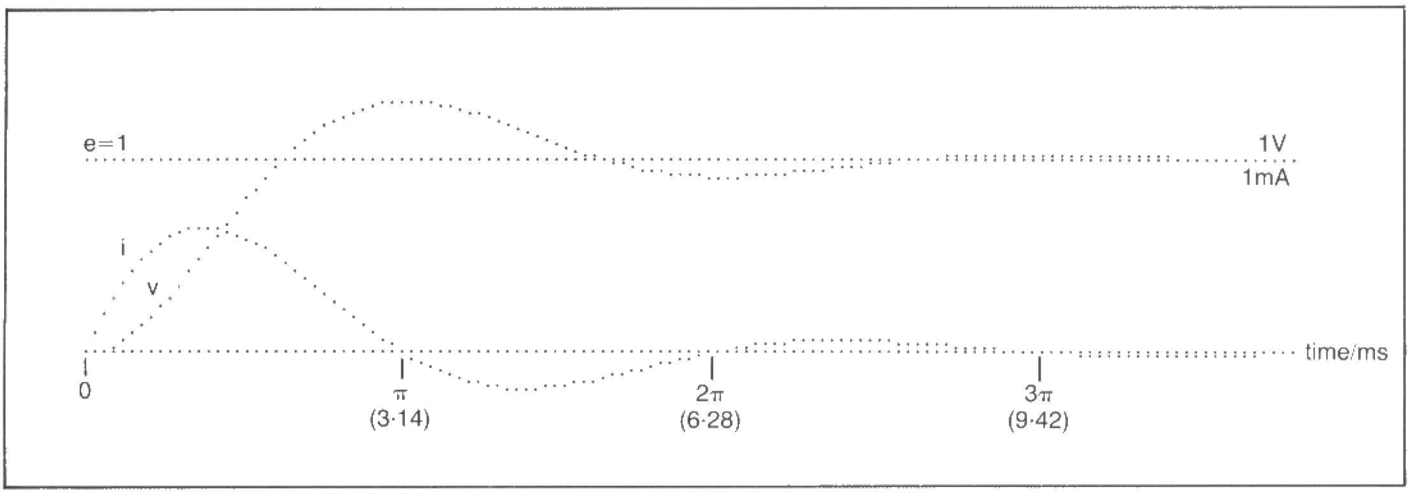


Figure 16. Predicted current and capacitor voltage for constant applied emf (time scale = $\omega_n t$). Damping factor = 0·4, natural frequency = 1000 rad/s.

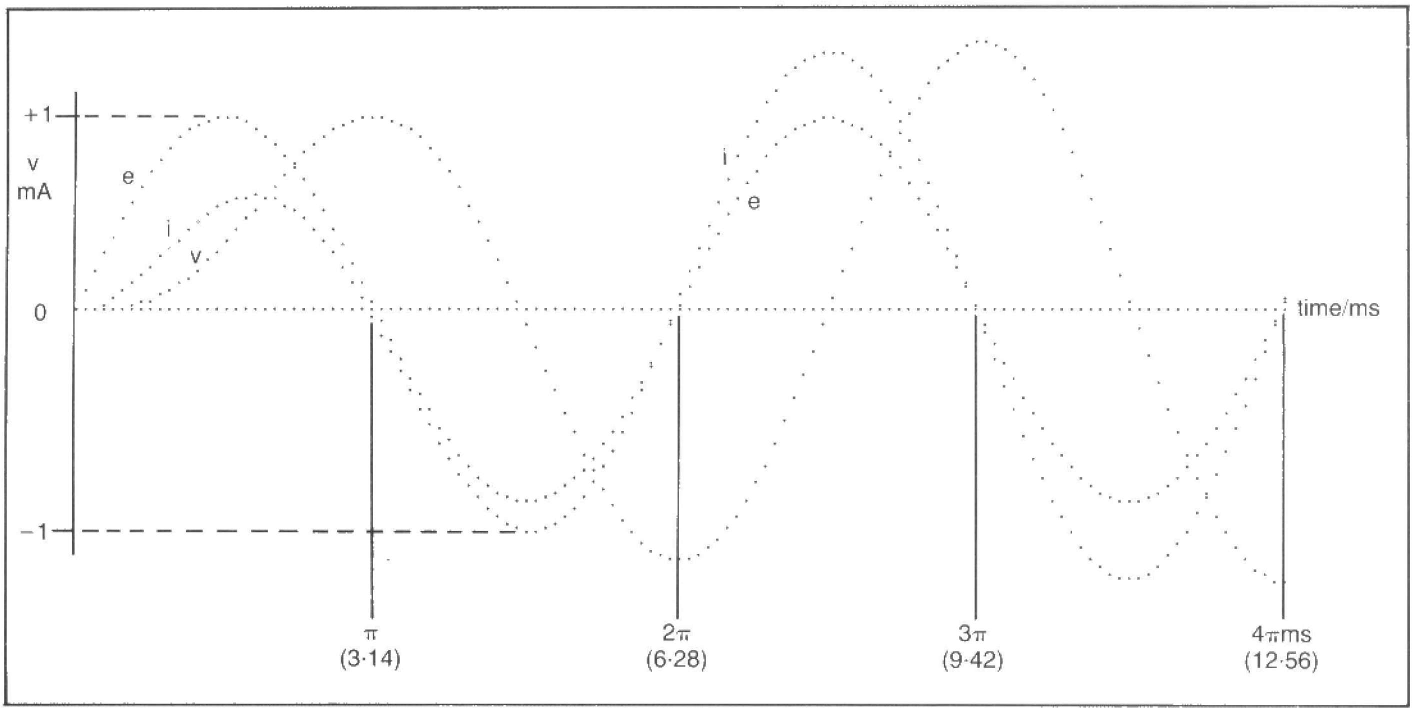


Figure 17. Predicted current and capacitor voltage for applied emf of 1 sin(1000t + Φ).

the capacitor potential (dv/dt). Hence the current and potential waveshapes can be predicted.

Program

The above rate of change equations can be evaluated for any input emf (e) using a computer and a suitable language. Note that the evaluation can be for *any* input waveshape, and that this is a good reason for considering this program.

The program is shown in Listing 9 (GW–BASIC) and Listing 10 (BBC BASIC). This program predicts, at successive steps of time, the current i (in amps), and the capacitor potential difference v (volts), when the applied emf e (volts) is constant (DC), a ramp, a sinusoid or any other waveshape. The predicted waveshapes are described in the next section.

The program is based on a FOR... STEP...NEXT loop, and contains several very interesting statements. In line 90, time is stepped from 0 up to 12·6ms, in intervals of h milliseconds, in order to evaluate the equations (h has to be relatively 'small', at present h=0·1ms). In line 100, the applied emf is specified as a constant; this is easily changed to a ramp, a sinusoid or any other waveshapes. Line 140 contains the 'rate of change' equations, evaluated as amperes per second and volts per second.

Line 170 has a method for predicting the changing quantity. It can be stated as: 'LET the new value become the old value plus an increment, where the increment is the product of the rate of change and a step in time.' Provided the step in time, h, is relatively 'small', then the predictions will be useful.

Waveshapes

Figure 16 shows the predicted waveshapes caused by a suddenly applied constant of +1. During the transient, the capacitor voltage exceeds the applied emf whilst the direction of the current actually reverses. The current and capacitor voltages both have a damped oscillation of 916 rad/s, which can be eliminated by increasing the resistance to 2000Ω.

These waveshapes, and the underdamped RLC circuit, can be described by two parameters; firstly, the natural frequency (ω_n = 1000 rad/s), and secondly, the damping factor (Z = 0·4). The frequency of the damped oscillation (ω_d = 916 rad/s) is always less than the natural frequency.

Note that the horizontal time axis is 12·6ms, which represents *two cycles* of the natural frequency. It is useful to think of time in terms of $\omega_n t$.

Figure 17 shows the waveshapes resulting from a sinusoidal input, with a frequency which is equal to the natural frequency of 1000 rad/s. Note that the steady-state current is in phase with the applied emf; this indicates that the circuit is behaving as a resistor (800Ω). Because of this effect, the natural frequency is also called the resonant frequency. The capacitor voltage (1·25V) is greater than the applied emf (1V), and lags it by 90°.

```
10 REM RLC Listing 1 PC version
20 REM Resistor-Inductor-Capacitor
30 REM Evaluate current and voltage
40 I=0 : V=0 : H=.0001 : SCREEN 2 : CLS
50 R=800 : L=1 : C=.000001 : REM R=2000
60 WN=1/SQR(L*C) : Z=(R/2)*SQR(C/L)
70 IF Z<1 THEN WD=WN*SQR(1-Z*Z) : REM E=1
75 IF Z<1 THEN P=1+EXP(-Z*3.142/SQR(1-Z*Z))
80 IF Z<.7 THEN WM=WN*SQR(1-2*Z*Z) : REM ss
85 IF Z<.7 THEN M=1/(2*Z*SQR(1-Z*Z))
90 FOR T=0 TO .0126 STEP H : X=T*50000
100 E=1   : REM 1000*T   1*SIN(WN*T+0) WM
110 PSET(X,100)                 : REM zero
120 PSET(X,100-E*50)            : REM volts
130 PSET(X,100-I*50000)         : REM amps
135 PSET(X,100-V*50)            : REM volts
140 SI=-R/L*I-1/L*V+1/L*E       : SV=+1/C*I
160 REM At time T+H secs : -
170 LET I=I+SI*H : LET V=V+SV*H : REM rates
180 NEXT T
```

Listing 9. The RLC prediction program written in GW-BASIC.

```
10 REM RLC Listing 2 BBC Acorn version
20 REM Resistor-Inductor-Capacitor
30 REM Evaluate current and voltage
40 I=0 : V=0 : H=1E-4 : MODE 4 : REM At T=0
50 R=800 : L=1.0 : C=1.0E-6 : REM R=2000
60 WN=1/SQR(L*C) : Z=(R/2)*SQR(C/L)
70 IF Z<1 THEN WD=WN*SQR(1-Z*Z) : REM E=1
75 IF Z<1 THEN P=1+EXP(-Z*3.142/SQR(1-Z*Z))
80 IF Z<.7 THEN WM=WN*SQR(1-2*Z*Z) : REM ss
85 IF Z<.7 THEN M=1/(2*Z*SQR(1-Z*Z))
90 FOR T=0 TO 12.6E-3 STEP H : X=T*1E5
100 E=1   : REM 1000*T   1*SIN(WN*T+0) WM
110 PLOT69,X,100)               : REM zero
120 PLOT69,X,E*100+200          : REM volts
130 PLOT69,X,I*100+200          : REM amps
135 PLOT69,X,V*100+200          : REM volts
140 SI=-R/L*I-1/L*V+1/L*E       : SV=+1/C*I
160 REM At time T+H secs : -
170 LET I=I+SI*H : LET V=V+SV*H : REM rates
180 NEXT T
```

Listing 10. The RLC prediction program written in BBC BASIC.

When the frequency of the applied emf is reduced to 825 rad/s, the steady-state current is reduced, but the capacitor voltage is increased to a maximum of 1·4V, with a lag of 64 degrees. Great care must be taken when discussing these effects.

There are four important frequencies:

the natural frequency, 1000 rad/s;
the damped natural frequency, 916 rad/s;
the resonant frequency, 1000 rad/s;
the peak frequency, 825 rad/s.

Note that the resonant frequency and the peak frequency refer to the frequency of the sinusoidal input emf.

Phasor Diagrams

A phasor diagram is used to represent a sinusoid, and is an alternative method of calculating the steady-state response. The phasor diagram shown in Figure 18 represents the waveforms at the moment when the current is zero (positive going), and when the frequency is equal to the natural frequency of the RLC circuit (1000 rad/s).

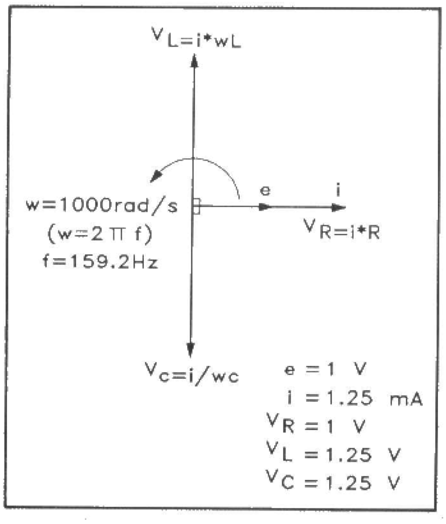


Figure 18. Phasor diagram for the RLC circuit at resonance. Current is in phase with the applied emf. Natural frequency = 1000 rad/s, damping factor = 0·4.

This moment in time – when the current is zero (positive-going) – is shown on Figure 17 at t = 6·28ms. The resistor volt drop is zero (positive-going), the capacitor potential is −1·25V (minimum), the inductor potential is +1·25V (maximum), and the input emf is zero (positive going). This situation repeats every cycle.

The phasors are based on the fact that the current sine wave leads the capacitor potential sinusoid by a quarter of a cycle, but lags the inductor potential sinusoid by a quarter of a cycle.

If the frequency of the applied sinewave is altered from the natural frequency of the RLC circuit, then the current will decrease. A lower frequency causes the current to lead the applied emf, whereas a higher frequency causes the current to lag the applied emf. Note that the capacitor potential difference (voltage) always lags the applied emf by 0 to 180 degrees.

Things to Do

It is left to the reader to change the value of the resistor (400, 800, 1200, 1600, 2000, 2400Ω), and predict a family of waveshapes for a constant input. These should be labelled with the appropriate value of the damping factor (Z).

Another interesting thing to do is to change the frequency of the applied emf, predict the waveshapes, construct the phasor diagram, and to measure the actual response using an oscilloscope.

Useful frequencies are ω_n, $\omega_n.10$ and $\omega_n/10$, where ω_n represents the natural frequency of 1000 radians per second. These are frequency 'decades' (alternatively use 'octaves'). If the damping factor (Z) is greater than 1, then the RLC circuit can be described by two 'break' frequencies. The frequency decades are then related to these break frequencies (see Bode diagrams in Part 2).

Finally

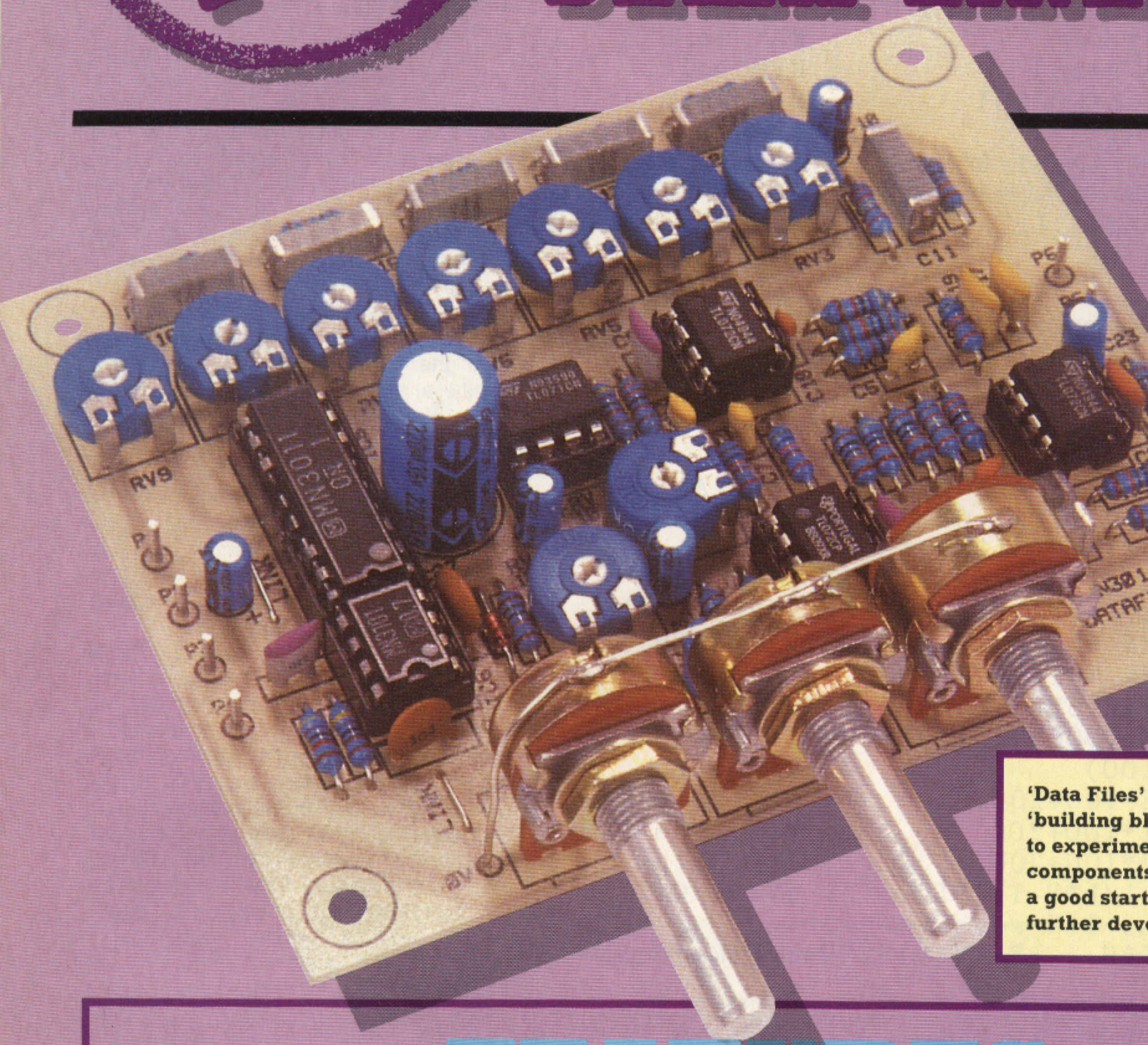
The Resistor-Inductor-Capacitor series circuit and a computer program have been used to explain how to predict the response waveshapes of the RLC circuit to any input, note ANY input. A damped oscillation has been predicted for a constant input (provided the value of the resistor is less than 2000Ω for the given values of L and C).

A sinusoidal response has been predicted for a sine wave input. At the natural frequency, the current is *in phase* with the applied emf, and the circuit is said to resonate. At certain frequencies the capacitor voltage is *greater* than the applied emf (provided the damping factor, Z, is less than 0·7). This is a very powerful method for predicting the dynamic responses of complicated systems using existing simulation programs.

Next time, we will move on to predicting impedance, current and capacitor charge potentials.

DATA FILE

MN3011 BUCKET-BRIGADE DELAY-LINE



'Data Files' are intended as 'building blocks' for constructors to experiment with and the components supplied provide a good starting point for further development.

FEATURES

★ **3328-STAGE AUDIO SIGNAL DELAY WITH 6 OUTPUT TAPS**
★ **SINGLE +15V SUPPLY** ★ **KIT AVAILABLE**

APPLICATIONS ★ **Reverberation Effect in Audio Equipment**
★ **Tremolo, Vibrato and Chorus Effects** ★ **Variable or Fixed Delay of Analogue Signals**

Introduction

The MN3011 is a 3328 stage bucket-brigade delay line with 6 tap outputs. Analogue signals, in the audio band, can be delayed by 1·98ms to 166·4ms by adjusting the clock frequency and making connection to the relevant output, see Table 1. Natural reverberation effects can also be produced by summing two or more of the six outputs. Figure 1 shows the IC pinout and Table 2 shows some typical electrical characteristics for the device.

Reverberation

Most electronic musical instruments (and acoustic instruments when played in a studio environment) are not based on sound created in a resonant room, and thus produce a 'flat' sound. Reverberation may be added by electronic means to add warmth to the sound of these instruments. A single pulse of sound (e.g. a handclap) will send a set of waves out across a room and, when they strike objects within the room, the direction and intensity of the sound waves will be changed. These changes in direction are caused by the sound waves being reflected, and it is these reflections that are the main cause of reverberation as the sound dies away. The attenuation and decay-time of the reverberation is determined

by the air and absorbent surfaces, see Figure 2.

All electronic systems used for adding reverberation depend on the same basic principle; the signal is delayed for a short time and part of it is fed back to the input. By carefully controlling the delay and amount of feedback, an effective 'reverb' can be produced. In reality, all that is being done is to recirculate a series of short echoes. If this is taken to extreme levels, oscillation results; this is hardly surprising when you consider that signals are being added, one on top of the other. However, when proper attention is paid to setting the levels, the sound can be quite realistic.

Figure 3 shows a simple reverberation unit based on 'bucket-brigade' memory. The memory is essentially a series of sample-and-hold circuits, each of which consists of an electronic switch and capacitor. The analogue signals stored in the capacitors are sampled under the control of a central clock signal. At each clock pulse the samples are shifted one capacitor to the right, hence the name 'bucket brigade' (the predecessor of today's fire brigade). However, a lifelike reverberation effect can only be achieved by using multiple delays of non-related durations.

Kit Available

A kit of parts including a high quality fibreglass PCB with screen printed legend is available to enable construction of a general purpose module based on the MN3011. Figure 4 shows the circuit diagram of the module and Figure 5 shows the block diagram; the PCB layout is shown in Figure 6.

Terminal No.	Symbol	Description
1	GND	
2	CP2	Clock pulse 2
3	V_{DD}	Supply voltage of −15V
4	OUT 6	Output of stage 3328 & 3329
5	OUT 5	Output of stage 2790 & 2791
6	OUT 4	Output of stage 1726 & 1727
7	OUT 3	Output of stage 1194 & 1195
8	OUT 2	Output of stage 662 & 663
9	OUT 1	Output of stage 396 & 397
10	CP1	Clock pulse 1
11	V_{GG}	Gate bias terminal
12	IN	Signal input terminal

Table 1. Terminal description.

The MN3011 has six different and non-related delays, while the attenuation of each of these is adjustable to give an optimum room simulation (RV4 to RV9). Recirculation of the echoes is

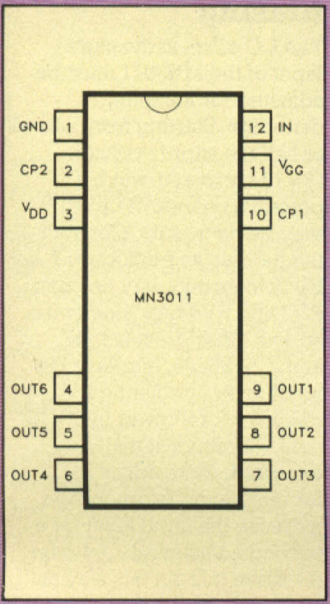


Figure 1. IC pinout.

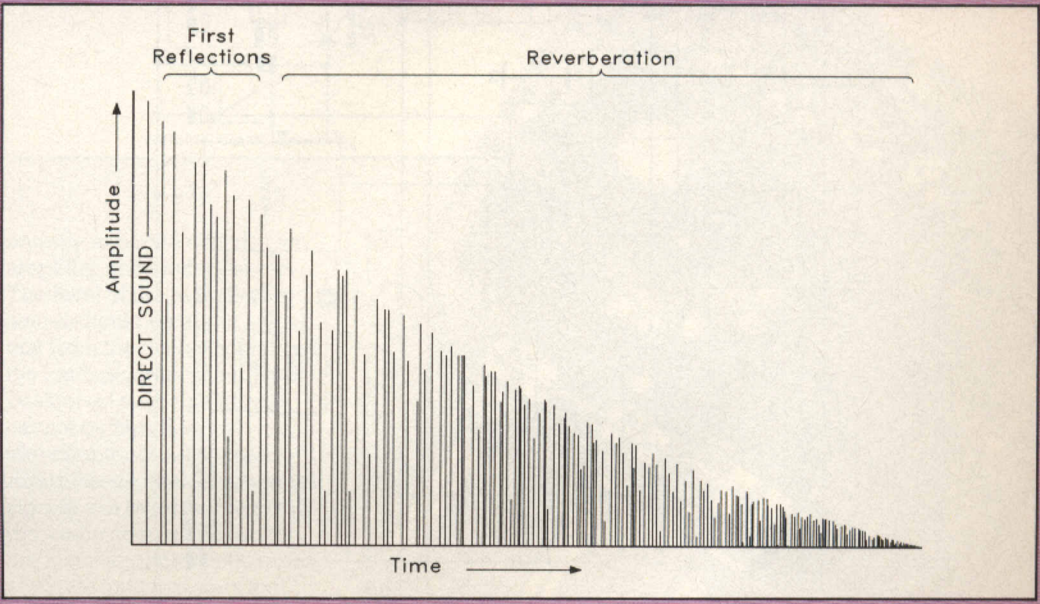


Figure 2. The profile of reflections of a single pulse of sound.

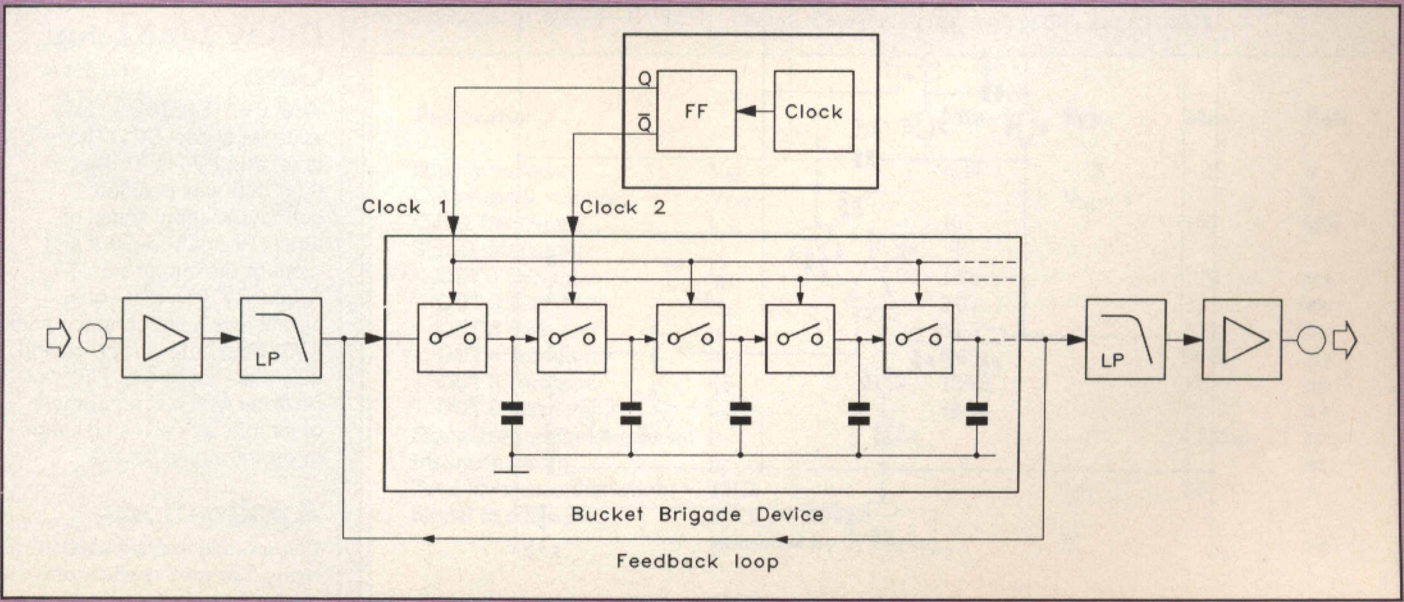


Figure 3. Block diagram of a simple BBD reverberation unit.

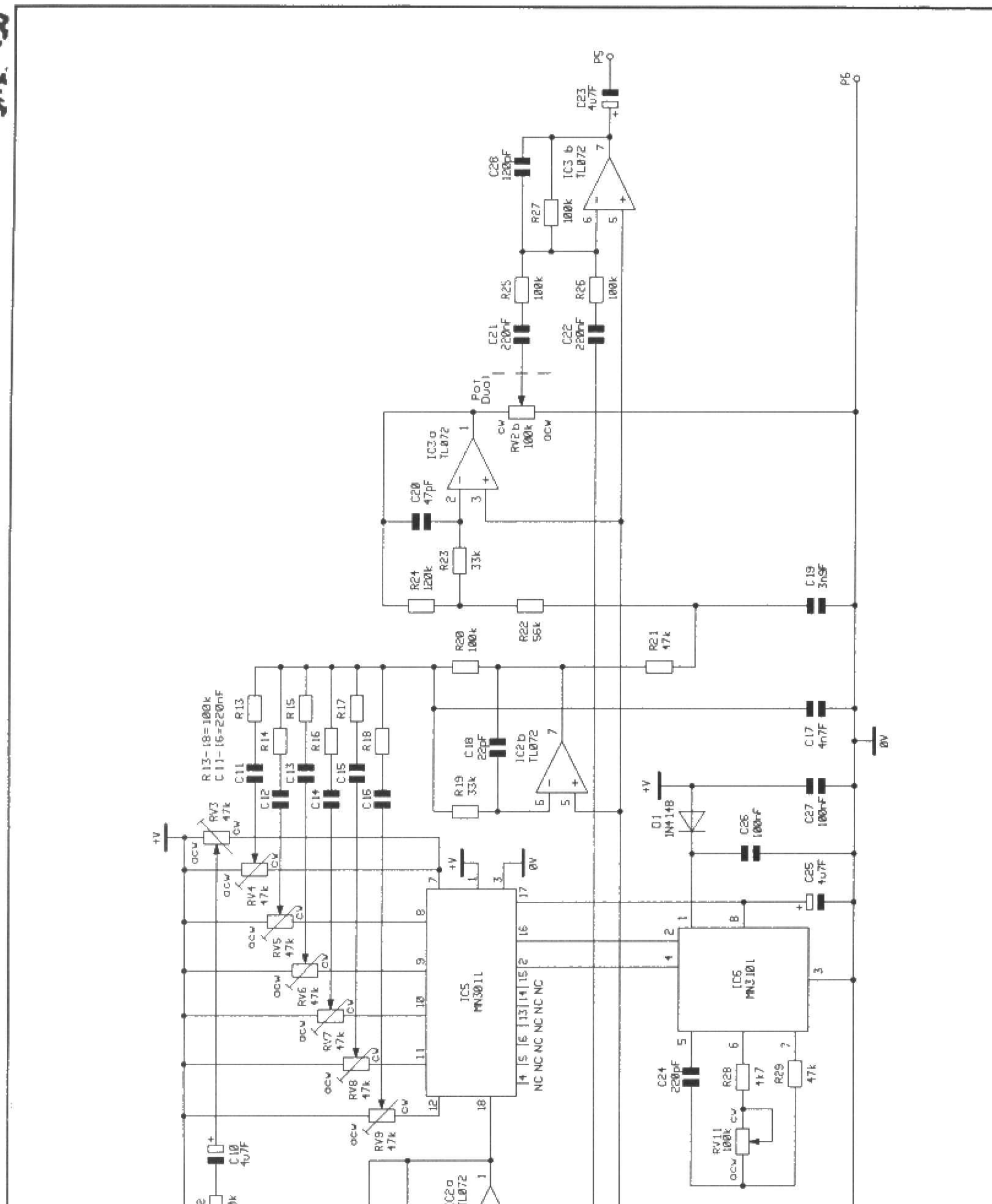


Figure 4. Module circuit diagram.

produced by feeding back part of the longest echo to the input (RV3).

The module requires a single +15V supply that is capable of delivering at least 40mA. It is important that the power supply is adequately smoothed and regulated to prevent any mains derived noise from entering the system via the supply rails. Power supply connections are made to P1 (+15V) and P2 (0V). Signals to the reverb unit are applied via P3 (input) and P4 (0V), and signals are output from the module via P5 (output) and P6 (0V). Figure 7 shows the wiring diagram. Note that the cases of RV1, 2 and 11 are connected to 0V through a wire link, see Photo 1.

Delay Line Biasing

The DC offset at the signal input of the MN3011 must be adjusted for minimum distortion. Starting from a level of half the supply voltage (RV12 set to mid-way), a potential change of up to 2V may be necessary. Connect the module as per Figure 7, set RV12 to its mid-way position, RV2 and RV4 fully clockwise, and all other presets fully anti-clockwise. Increase the input level by rotating RV1 clockwise, followed by RV10, until the output signal is distorted. Next, adjust RV12 for minimum distortion, and increase the input level for a second adjustment. Optimise the drive margin this way until no further improvement is noted.

Delay Line Loop Gain

With RV3 (Feedback) fully anti-clockwise, RV11 (Reverb time) and RV4 to RV9 set to their mid-way position, connect an input signal of about 1V peak-to-peak and monitor the output signal. Adjust RV10 so that equal output levels are obtained with RV2 (Mix) fully clockwise and fully anti-clockwise. This can be done with test equipment or simply 'by ear' using a tape or digital signal source.

Applications

The module may be used in many different applications requiring a natural reverb effect, or even a single or

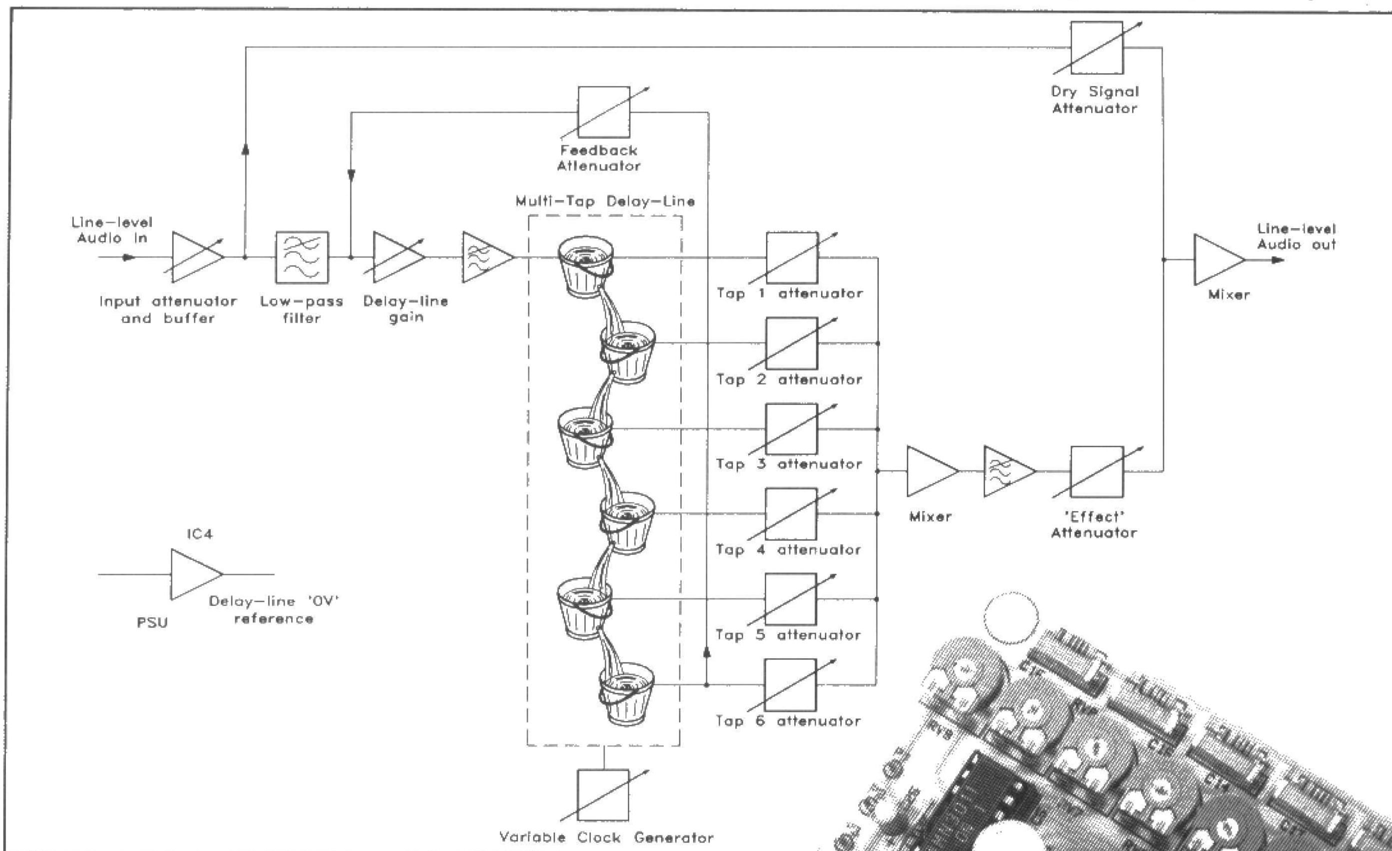


Figure 5. Module block diagram.

multiple delay of up to 166ms using only one of the tapped outputs from the MN3011.

Audio signals, on entering the module, are split into two paths, which are re-united near the output. The simplest of these paths is a direct link from the input of the module to the output mixer stage (RV2a and IC3b); the second path is via the MN3011 delay line. RV4 to RV9 set how much signal is mixed from each of the six tapped outputs from the MN3011 and sent to the output, and RV3 controls the amount of echo sent back for recirculation.

Note that, as the MN3011 clock frequency must be at least 3 times the maximum input signal frequency, the delayed signal has a limited bandwidth of 3·3kHz. This bandwidth restriction is of little consequence to the audible results since the higher frequencies in a 'live' environment are quickly absorbed and do not, therefore, reverberate.

Applications for this module include adding reverb to a domestic hi-fi environment, thus recreating the 'spaciousness' or reverberation experienced in a concert hall or theatre. For example, the system could be entirely separate with its own amplifier and loudspeakers. The level of the reverberated sound should be about half of that from the main system, and the loudspeakers should be positioned such that they cannot be heard as an identifiable sound source. Alternatively, the reverberated signals can be mixed with the dry audio source and fed to the main amplifier. In this case, separate loudspeakers and amplifier are not necessary.

By varying the delayed/ reverb signal mix (RV4 – RV9),

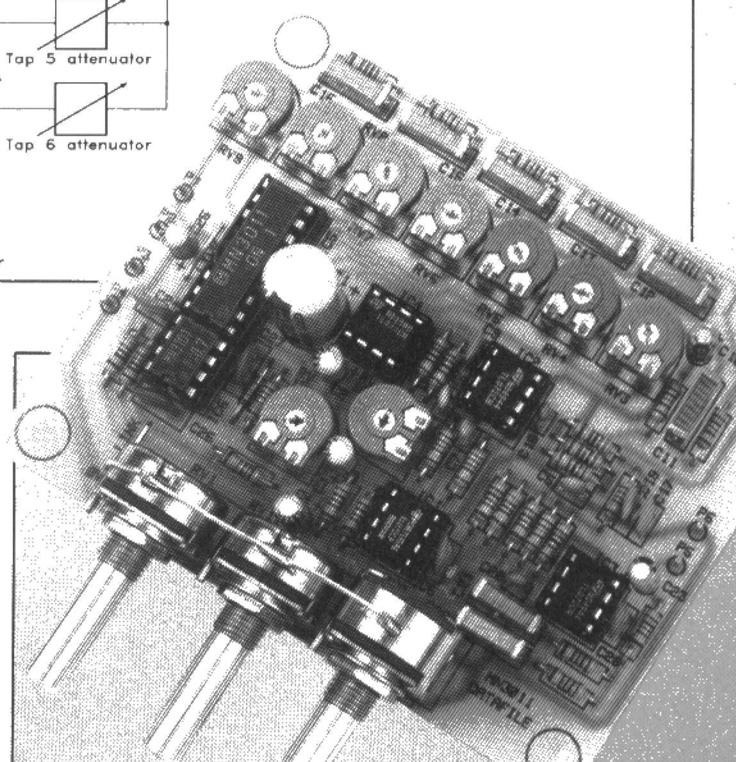


Photo 1. Connecting the cases of RV1,2 and 11 to 0V.

Parameter		Min.	Typ.	Max.	Unit
Supply voltage:	V_{DD}	−14	−15	−16	V
Gate supply voltage:	V_{GG}		$V_{DD}+1$		V
Clock frequency:	f_{CP}	10		100	kHz
Signal delay time					
OUT 1 Terminal:	t_{D1}	1·98		19·8	ms
OUT 2 Terminal:	t_{D2}	3·31		33·1	ms
OUT 3 Terminal:	t_{D3}	5·97		59·7	ms
OUT 4 Terminal:	t_{D4}	8·63		86·3	ms
OUT 5 Terminal:	t_{D5}	13·95		139·5	ms
OUT 6 Terminal:	t_{D6}	16·64		166·4	ms
Signal frequency response:	f_i			$0{\cdot}3xf_{CP}$	kHz
Insertion loss:	L_i	−4	0	4	dB
Total harmonic distortion:	THD		0·4	2·5	%
Signal to noise ratio:	S/N $f_{CP}=100$kHz weighted by 'A' curve		76		dB

Table 2. Typical electrical characteristics.

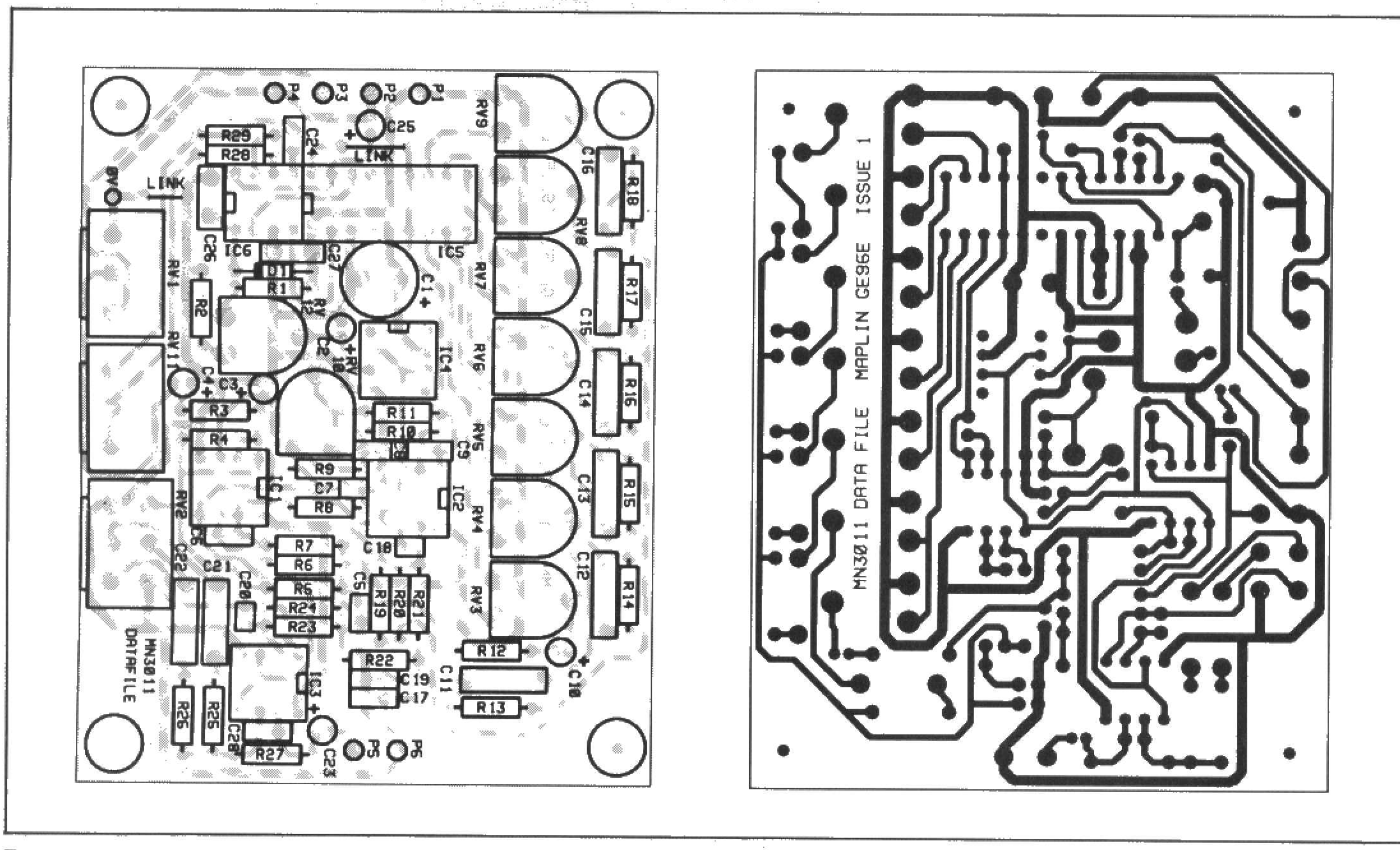


Figure 6. PCB legend and track.

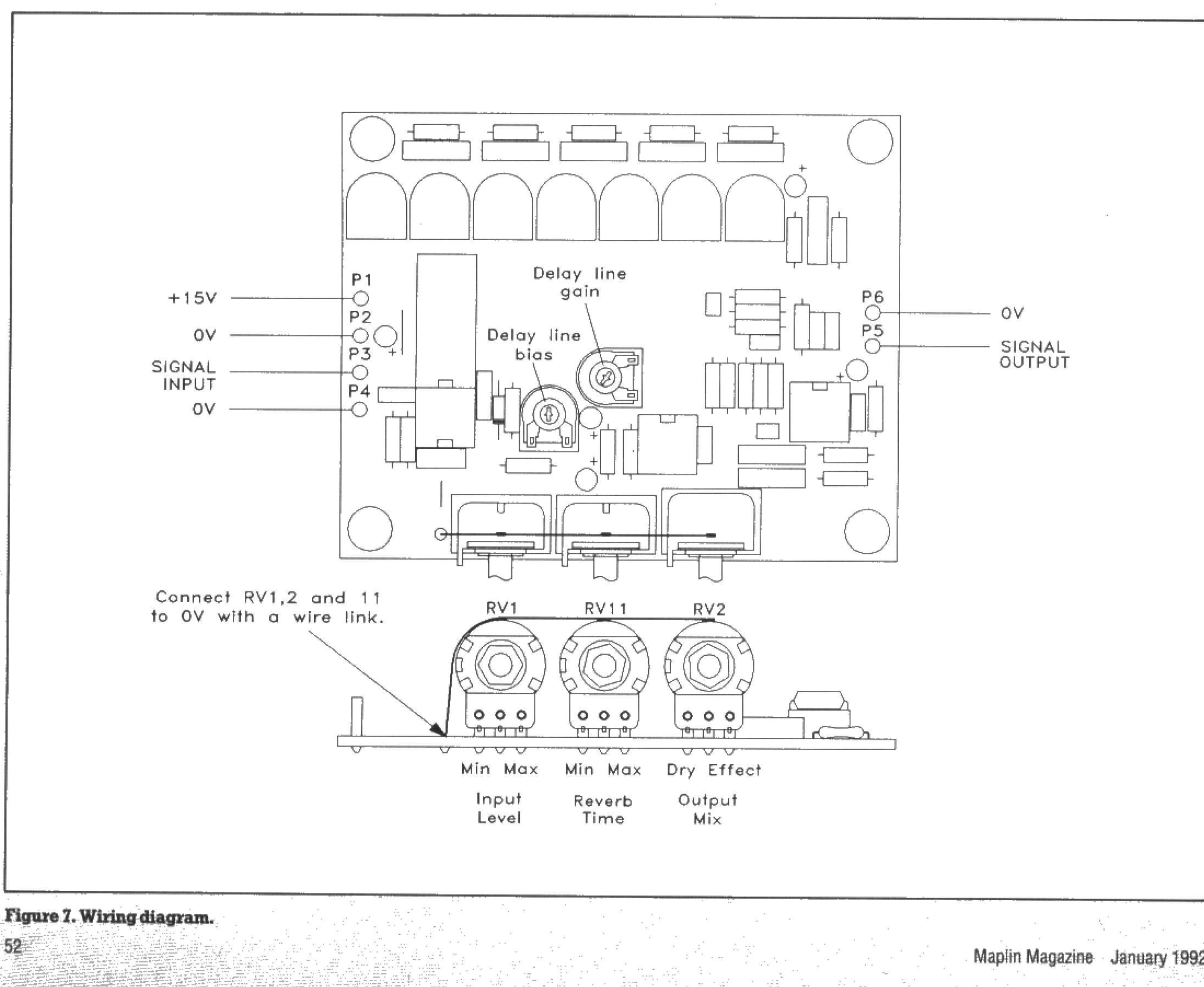


Figure 7. Wiring diagram.

feedback (RV3), reverb time (RV11) and mixture of direct and delayed/reverberated signals (RV2), a variety of interesting effects can be obtained. Here are a few ideas to try:

With equal levels of only one delay tap and direct signals, coupled with a few milliseconds of delay, a 'double-tracking' effect is produced. This makes a single input sound like a pair of independent, but time-synchronised, outputs. By adding the delayed signals of further tap outputs the duet can be turned into a quartet, or even an octet, etc.

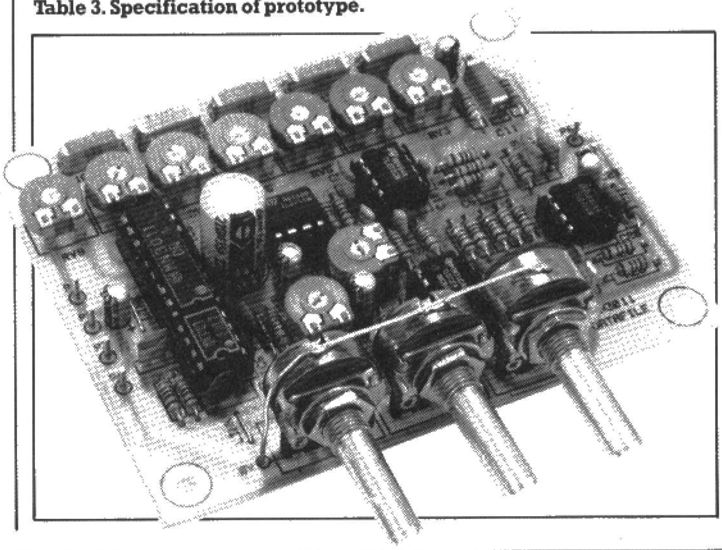
When equal levels of direct and a mix of delayed signals are used with a long reverb time, and almost maximum feedback, the sounds seem as if they are being played in a large cathedral. The apparent dimensions of this 'chamber' can be varied through the reverb-time control, while the 'hardness' of the chamber can be altered by the feedback control. The sounds can be varied from those of a large cavern, down to a well-furnished lounge.

When equal levels of mixing are used with a short reverb time and a small quantity of feedback, the impression is given that all sounds are being played inside a small, hard-faced pipe. The size of the 'pipe' can be altered with the reverb-time control and the hardness of the pipe is variable through the feedback control, allowing sounds to be varied from those of a sewer pipe to a bucket.

Finally, Table 3 shows the specification of the prototype MN3011 module.

Parameter	Min.	Typ.	Max.	Unit
Supply voltage:	14	15	16	V
Supply current:		40		mA
Input signal level (RV1 & RV2 fully clockwise):		1	2·5	Vrms
Input signal level (RV1 fully clockwise, RV2 fully anti-clockwise):		1	8	Vrms
Input impedance:		47		kΩ
Delay time:	1·7		160	ms
Dry signal path frequency response:	7		23k	Hz
Delay signal path frequency response:	8		3·3k	Hz
Output signal level:		1		Vrms
Output impedance:		600		Ω

Table 3. Specification of prototype.



MN3011 BUCKET-BRIGADE DELAY-LINE PARTS LIST

RESISTORS: All 0·6W 1% Metal film (Unless specified)

R1,2	150k	2	(M150K)
R3,4,5,7, 13-18,20,25-27	100k	14	(M100K)
R6,11,21,29	47k	4	(M47K)
R8,9,22	56k	3	(M56K)
R10,19,23	33k	3	(M33K)
R12	220k	1	(M220K)
R24	120k	1	(M120K)
R28	4k7	1	(M4K7)
RV1	Min Pot Log 47k	1	(JM78K)
RV2	Min Dual Pot Lin 100k	1	(JM82D)
RV3-9	Hor Encl Preset 47k	7	(UH05F)
RV10	Hor Encl Preset 470k	1	(UH08J)
RV11	Min Pot Lin 100k	1	(JM74R)
RV12	Hor Encl Preset 100k	1	(UH06G)

CAPACITORS

C1	PC Elect 220μF 35V	1	(JL22Y)
C2,4,10,23,25	Minelect 4μ7F 35V	5	(YY33L)
C3	Minelect 10μF 16V	1	(YY34M)
C5	Ceramic 1n5F	1	(WX70M)
C6,9,24	Ceramic 220pF	3	(WX60Q)
C7	Ceramic 680pF	1	(WX66W)
C8	Ceramic 1n8F	1	(WX71N)
C11-16,21,22	Poly Layer 220nF	8	(WW45Y)
C17	Ceramic 4n7F	1	(WX76H)
C18	Ceramic 22pF	1	(WX48C)
C19	Ceramic 3n9F	1	(WX75S)
C20	Ceramic 47pF	1	(WX52G)
C26,27	Minidisc 100nF 16V	2	(YR75S)
C28	Ceramic 120pF	1	(WX57M)

SEMICONDUCTORS

D1	1N4148	1	(QL80B)
IC1,2,3	TL072	3	(RA68Y)
IC4	TL071	1	(RA67X)
IC5	MN3011	1	(UM65V)
IC6	MN3101	1	(UM66W)

MISCELLANEOUS

P1-6	Pins 2145	1 Pkt	(FL24B)
	DIL Socket 8-pin	5	(BL17T)
	DIL Socket 18-pin	1	(HQ76H)
	PCB	1	(GE96E)
	Instruction Leaflet	1	(XT23A)
	Constructors' Guide	1	(XH79L)

The Maplin 'Get-You-Working' Service is not available for this project.
The above items are available as a kit, which offers a saving over buying the parts separately.
Order As LP80B (MN3011 BBD Reverb Kit) Price £38.95
Please Note: where 'package' quantities are stated in the Parts List (e.g. packet, strip, reel, etc.) the exact quantity required to build the project will be included in the kit.

The following new item (which is included in the kit) is also available separately, but is not shown in the 1992 Maplin Catalogue.
MN3011 BBD Reverb PCB **Order As GE96E Price £3.75**

Stray Signals

by Point Contact

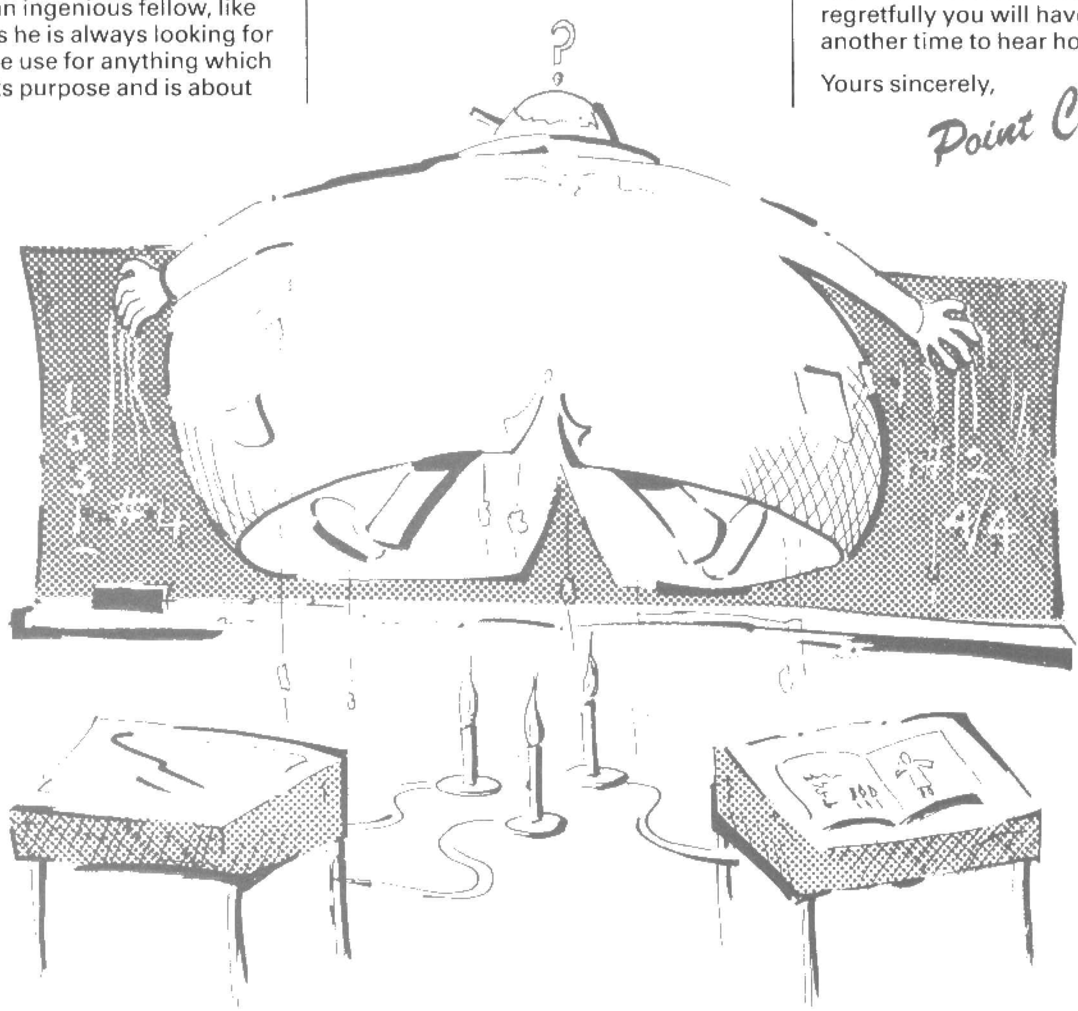
I see that the UK subsidiary of a well-known American electronics firm is selling dummy SMT (surface mount technology) components. You might think the idea was to make dummy wrist-watch transistor radios, for sale to dummy consumers, but actually there is a serious end purpose in view. They are used for pre-production trials of newly installed surface mount PCB assembly machines, machines with a tremendous throughput and a voracious appetite for components. Feeding them real ones would soon prove very expensive, whereas the dummies are physically just like the real thing but cost very much less. All types from resistors through SOT23, 44 pin PLCC and even 100 pin gull-wing packages are available. After all, if a manufacturer has gone to the expense of having an SMT assembly machine installed, he is going to want the vendor to prove that it works – that the controller for the pick-and-place, the preheating, the solder bath and all the other stages has all its parameters properly set to ensure a reliable product and no waste.

Your average electronic engineer is an ingenious fellow, like the Wombles he is always looking for an alternative use for anything which has served its purpose and is about to be thrown away. I recall an experiment with a mini hot-air balloon, namely the extremely light plastic bag covering my suit when it came back from the cleaners. With the hole at the top where the wire hanger used to poke through sealed with Sellotape, a colleague (at the labs where Point Contact worked as a new graduate) held it upright, another held the bottom open whilst PC played the flame from one of the then new-fangled butane blow torches up inside. The bag soon ballooned out promisingly, and on letting it go shot up eagerly, only to turn turtle, spilling out all the hot-air. Clearly it needed some ballast at the bottom to keep it right way up. A few paper clips proved too light, it still turned turtle, so we hung some wirewound resistors onto them. These 'load resistors' were an instant success – after refilling the contraption with hot-air it shot straight up to the very high ceiling of the lab. There it rested for ages, only deigning to drift slowly down again a quarter of an hour later as the Managing Director was passing through the lab, whilst we all pretended not to notice.

Now the uncle of a colleague of mine, at these same labs, was in the plastics production machinery business. His job was installing, among other things, machines for producing three foot wide 'layflat tubing', and naturally setting up, testing and demonstrating to the customer that everything was working satisfactorily resulted in miles of surplus tubing. Nevertheless, this exercise was just as essential as with the SM PCB machinery mentioned earlier. Clearly, we thought, there ought to be a use for a copious free supply of the stuff, so a group of us got together to go into the hot-air balloon business. Slitting the tubing down the side resulted in a sheet of light to medium gauge polythene six feet wide and as long as you liked. PC volunteered the use of his loft and an old electric iron, and we experimented. With a length of hardboard on edge, two layers of polythene covered with brown paper and a deft hand with the iron, we conquered the technique of heat sealing seams and reckoned we were ready to design and make a decent sized hot-air baloon. Our calculations indicated that for a goodly amount of lifting power, not exactly man-carrying but much more impressive than just a few resistors, five or six panels ten feet long should do the trick. Unfortunately however, I seem to have run out of space, so regretfully you will have to wait until another time to hear how we got on.

Yours sincerely,

Point Contact



All You Need to Build Your Own

FUN TRONICS PROJECT No2

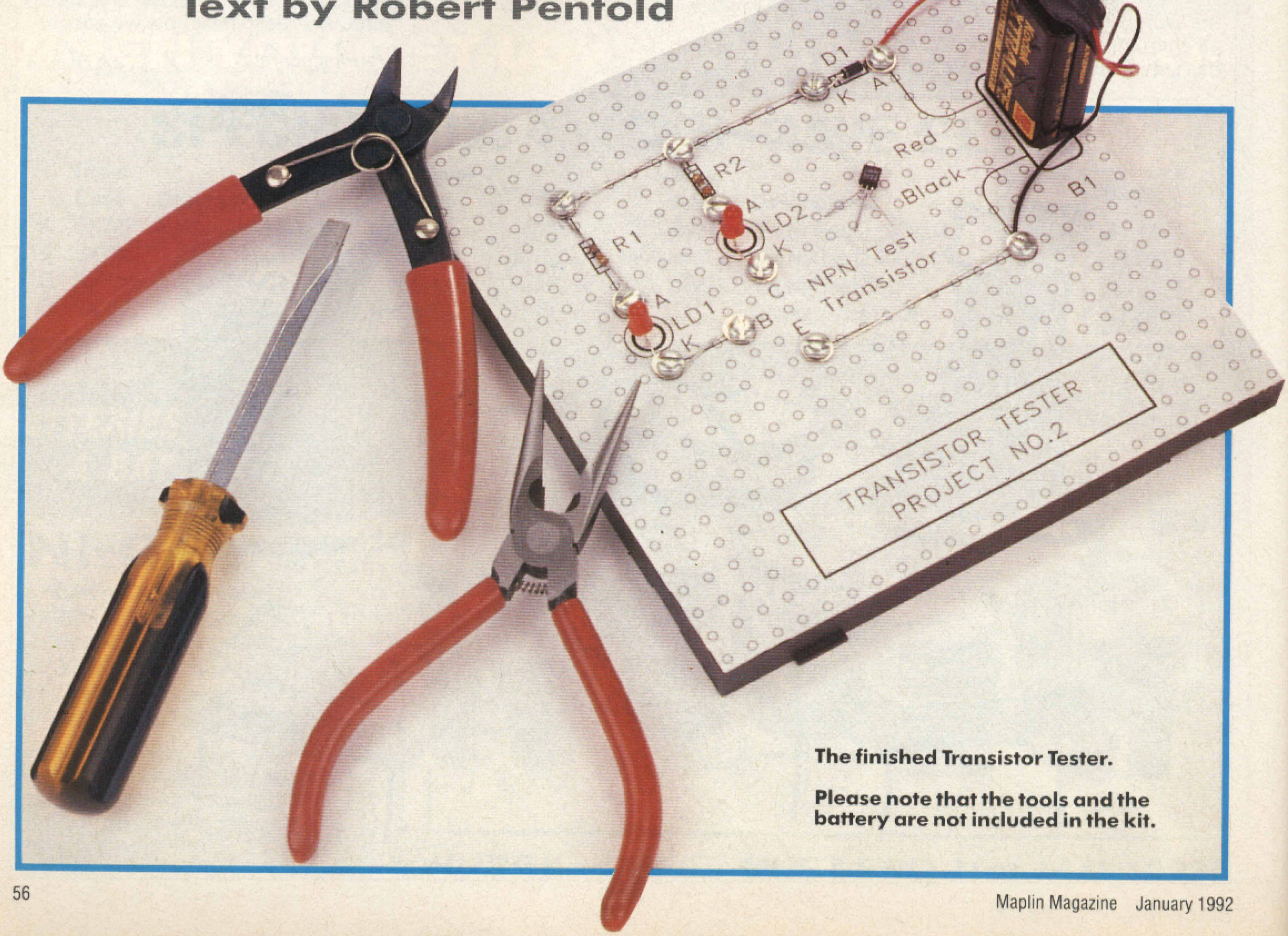
TRANSISTOR TESTER

Text by Robert Penfold

This is the second in a series of easy-to-build electronics projects for complete beginners, who require a simple and fun starter to electronic project building. These projects are ideal for the young person as no soldering is needed. All the projects are built on the same type and size of plastic 'peg- board'. The only tools needed to build this project, and others in the series, are a pair of wire cutters/strippers and a small screwdriver; a pair of pliers would also be useful.

This Month's Project

As well as showing you how a transistor works, this handy kit allows you to test any transistors that you may use in your own projects. It will test small and medium power transistors (the types in small plastic and metal cases), which means it can test most of the transistors you are likely to use. Like most of the transistor testers you can buy in the shops, it may not always work properly with high power transistors (those which have large cases with one or two fixing holes). Normally this kind of transistor will



The finished Transistor Tester.

Please note that the tools and the battery are not included in the kit.

only work properly at fairly high power levels which this tester cannot provide.

In the world of electronics there are two basic types of transistor used in most circuits, known as 'NPN' and 'PNP' types. The two are similar in the way they work, and differ only in that one needs the power supply connected one way round, while the other type needs the supply connected the opposite way round. This tester is designed to check NPN transistors, which are used much more than the PNP variety. However, as we shall see later, the circuit can easily be changed so that it can test PNP transistors.

How it Works

Figure 1 (known as a circuit diagram) shows the parts of the project and how they are connected together, the circuit diagram is the NPN version of the unit. The basic action of a transistor is to provide a large flow of electricity through its collector ('C') lead if a small current flows through the base ('B') lead. For a typical transistor the flow of electricity through the collector is about 100 or 200 times that flowing through its base lead. In other words, it 'amplifies' the input signal that was applied to its base by about 100 or 200 times. Some transistors give more amplification than this (up to about 1000 times). A few transistors give very little amplification, only about 20 times.

In this circuit R1, a resistor, is fitted to make sure that the electric current flowing through the base terminal of the transistor is suitably small. This current flows through LD1 which is a light emitting diode (LED for short).

The current is just enough to produce a visible glow from LD1, but it will be rather dim. LD2, another LED, is connected so that it receives the higher current which flows through the collector lead of the test transistor. Resistor R2 limits the maximum current that can flow, to a safe level. This protects both LD2 and the test transistor from being damaged. The diode D1, will allow the current in the circuit to flow in one direction only. This diode will 'block' the supply (and so protecting the circuit), should the battery be accidentally connected the wrong way round.

Figure 2 shows the circuit diagram for the unit when it is set up to test PNP transistors. Several changes have to be made from the NPN test circuit, however. Not only does the battery have to be connected the other way round, but the connections to D1 must be also swapped over, otherwise this

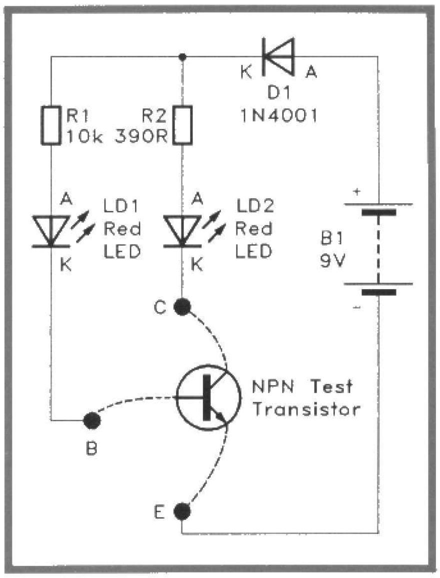


Figure 1. The Transistor Tester circuit diagram (for NPN transistors).

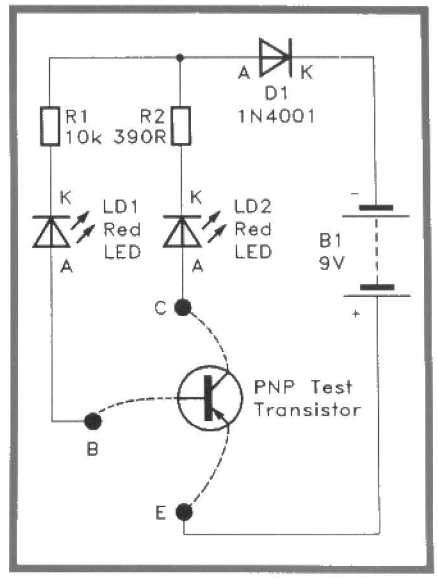


Figure 2. The Transistor Tester circuit diagram (for PNP transistors).

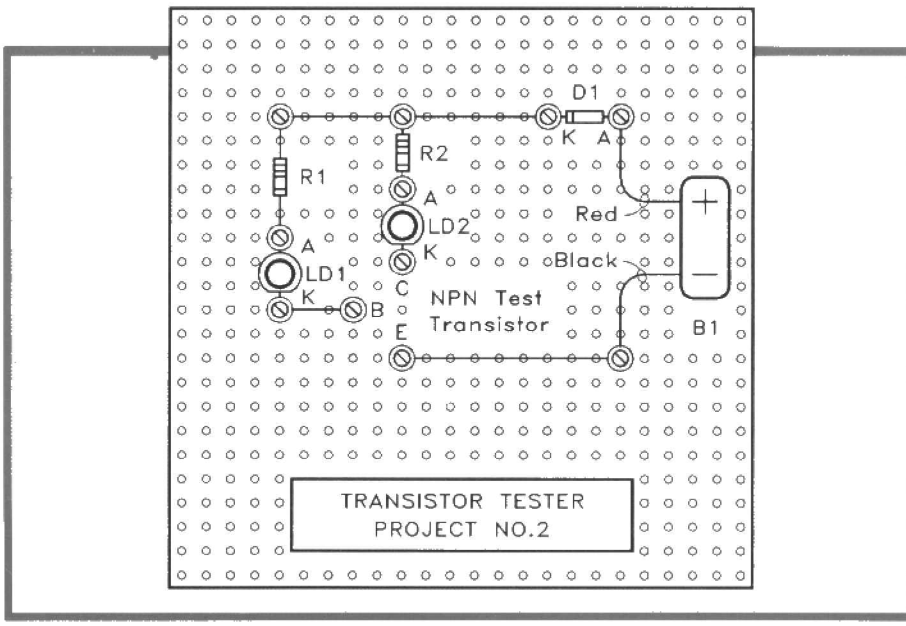


Figure 3. The component guide-sheet for the Transistor Tester.

component would block the current from the battery. In addition, the connections to each of the LEDs must be swapped over. The LEDs are not small light bulbs, but diodes, similar in the way they work to D1, as they allow the current to pass in one direction only. If they are not connected the right way round, no current will flow, and the LEDs will not light up.

Getting it Together

Firstly, read through this section and then *carefully* follow the instructions, one step at a time. Refer to the photographs of the finished project if this helps.

1. Cut out the component guide-sheet provided with the kit (which is a full-size copy of Figure 3), and glue it to the top of the plastic board. Paper glue or gum should be okay. Do not soak the paper with glue, a few small 'dabs' will do.

2. Fit the link wires to the board using the self-tapping screws and washers provided. The link wires are made from bare wire. Loop the wire, in a *clockwise* direction around each screw to which it must connect, taking the wire under the washers. Do not fully tighten a screw until all the leads that are under it are in place, and do not over-tighten the screws, otherwise the plastic board may be damaged.

3. Recognise and fit the components, in the order given below, using the same method as for the link wires. Cut the components' wires so that they are just long enough to loop around the screws; otherwise long leads left flapping around may touch each other (this is known as a 'short-circuit') and may stop your circuit from working.

a) The first components to be fitted are Resistors R1 and R2. These are small sausage-like components having a leadout wire at each end, and several coloured bands around their bodies. For R1 these colours

are brown, black, orange, and gold. The colours for R2 are orange, white, brown, and gold. These first three bands tell us the value of the resistor. R1 has a value of 10,000 ohms, which is often written as 10 kilohms, or 10kΩ for short. R2, however, has a value of 390 ohms, written as 390Ω or 390R for short. The fourth band tells us how near to the given value the resistor is likely to be. This fourth band is known as the 'tolerance' band. Unlike diodes or transistors, it does not matter which way round resistors are connected.

b) Next fit the LEDs, LD1 and LD2, which are both of the same type. Each is a 'blob' of clear red plastic, with two wires coming out of one end. They are fitted in the positions shown on the guide-sheet, and *must* be connected the right way round – or they will not light up. One side of each LED is flattened (the lead on this side of the LED is known as the cathode (K), while the lead on the other rounded side, is called the anode (A)). The LED, the circuit symbol and connections are shown in Figure 4. Make sure that the LEDs are fitted so that the 'flattened' sides line up with the drawing of the LED printed on the guide-sheet.

c) The next component to be fitted is D1, which is a small tube-like component having a lead at each end of its black body. Like LD1 and LD2, it must be connected the right way round, (in other words, D1 is a 'polarised' component). Its 'polarity' is indicated by a white (or silver) band close to one end of the body, which tells us the way in which it must be positioned. D1, its circuit symbol and connections, are shown in Figure 5. The diode should be fitted so that the band lines up with the band on the drawing of the diode on the guide-sheet.

d) Last of all fit the battery connector and battery, B1; the connector must be attached to the board with its coloured leads the correct way round.

The battery connector has two press-stud clips on a piece of plastic, and two wires coming from it coloured red and black. The red and black leads should be connected as shown on the layout sheet. The 9V PP3 type battery should be connected to the battery connector, it will only fit properly one way round.

Testing and Use

To check that the unit is working, use a piece of left-over wire to temporarily connect together the 'B' and 'E' test terminals on the board. This should result in LD1 glowing dimly, and you might need to shade it from any bright lights in order to see that it has lit up. Next,

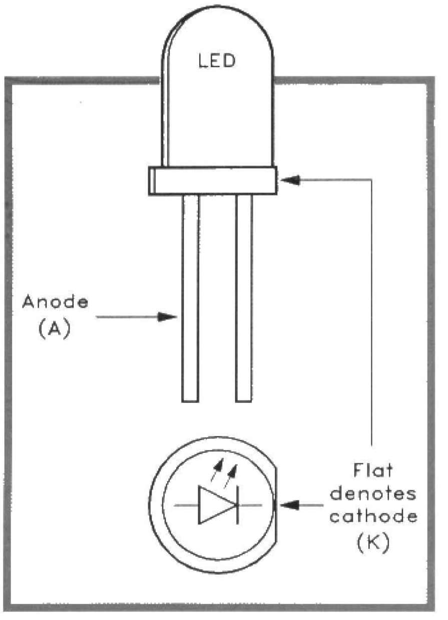


Figure 4. LED symbol and connections (LD1, LD2).

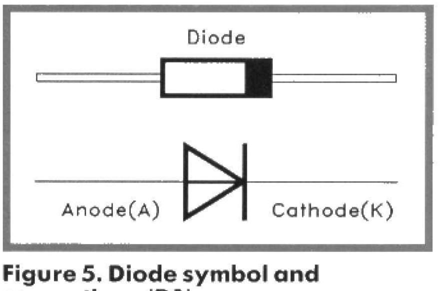


Figure 5. Diode symbol and connections (D1).

temporarily connect together the 'C' and 'E' terminals. This second test should cause LD2 to glow more brightly. If either, or both, diodes fail to light up, check that the battery and three diodes are all connected the right way round. Also check that all wires are properly held in place by the screws and washers.

Two test transistors are included in the kit. One is marked 'BC548', or something very similar, this is the NPN test transistor. The other one is a PNP type, and is marked 'BC558', or something very similar. Figure 6 shows the circuit symbols for NPN and PNP transistors, and it also shows which lead is which for the two test transistors. This should make it easy to get the test transistor connected correctly. Take the NPN transistor, and connect its collector and emitter leads to the appropriate terminals of the tester. There is no need to fix it in place – simply hold it with the leads touching the two terminals.

With the base lead not connected, neither of the two LEDs should light up. If LD2 lights up, this indicates that the test device is 'leaky'. This means that current is 'leaking' through the collector-emitter part of the transistor, completing the circuit and causing the LED to glow. Alternatively, you might have connected it wrongly.

Now touch all three leads of the transistor onto the correct terminals of the tester. LD1 should light up dimly, and LD2 should light up brightly, indicating that the test transistor is providing a useful amount of current amplification. If LD2 only lights very dimly, or not at all, the test component is providing little or no amplification. In other words, it is no good.

Before the PNP transistor can be tested you must remove and reconnect LD1, LD2, D1, and B1 the other way round. Apart from this, the test procedure is the same for both NPN and PNP transistors.

Note that not all transistors have the leadout arrangement shown in Figure 6. Even transistors which look just like the sample transistors might have the leadouts in a different order. A transistor data book will provide leadout details for a wide range of transistors, as does the 'semiconductor' section of the Maplin catalogue. Incidentally, the word 'semiconductor' refers to a wide range of components which include transistors, diodes and integrated circuits (ICs or 'chips').

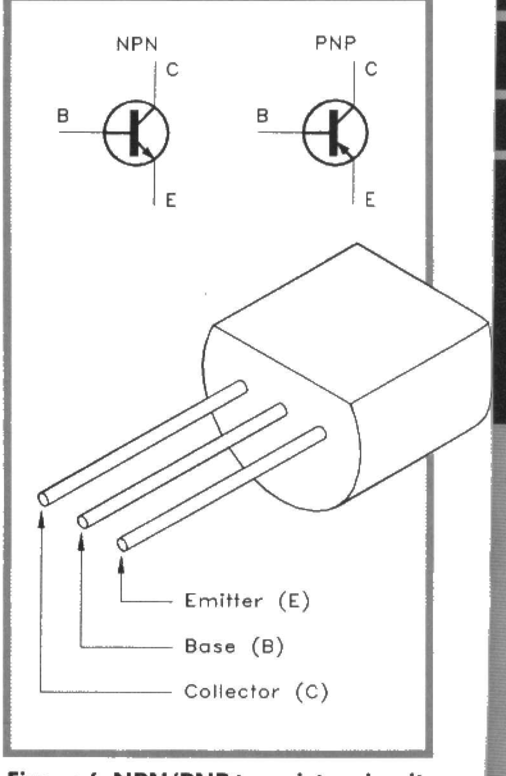


Figure 6. NPN/PNP transistor circuit symbols, and transistor lead identification.

Other Uses

This project can also be used as a diode tester. If a diode is connected across the 'C' and 'E' terminals, connecting it one way round will result in LD2 lighting up, while connecting it the other way round will result in LD2 remaining unlit.

Availability

The Funtronics Transistor Tester is available from Maplin Electronics, through our chain of regional stores, or by mail order, Order Code LP86T Price £2.95.

MICRO-COMPUTER TESTING & FAULT FINDING

by Alan Pickard

Part Two – Input and Output Devices

In Part 1 we looked at a single block diagram representation of a microcomputer which included an input device (keyboard) and an output device (monitor). In this article we will take a closer look at how these two devices are interfaced/connected to the microprocessor and what basic knowledge is needed to have an understanding of their operation from an investigative or fault-finding nature. For completeness, memory devices (already mentioned in Part 1) will be described at the end of this article.

Input/Output Circuits

An input device, such as a keyboard, is not connected directly to a microprocessor data bus, but requires intermediate logic circuitry and buffering. Most interface circuits are based on 40-pin VLSI devices which belong to the same 'family' as the MPU, or are at least compatible with it. An example of an interface chip in the 6502 MPU family is the 6522 Versatile Interface Adaptor (VIA). The associated data sheet for this device details its operation and how it may be programmed for a particular operation. Figure 1 shows the principle of operation.

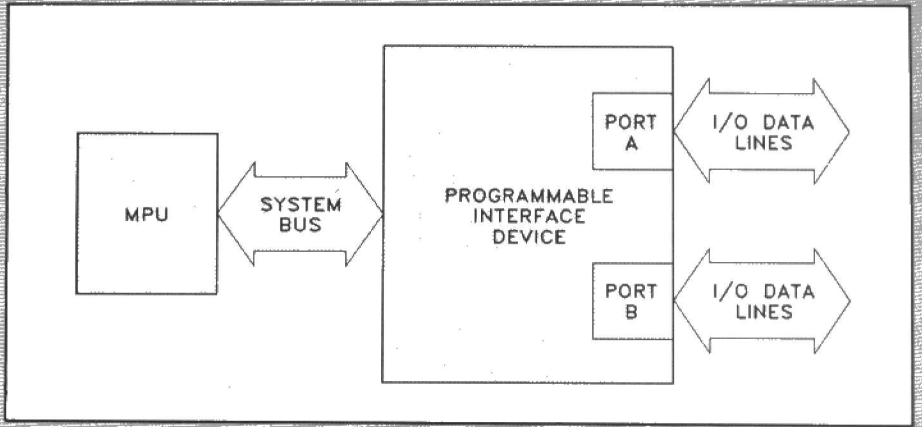


Figure 1. Principle of I/O interfacing.

The 6522 contains two 8-bit ports which can be programmed to function as inputs or outputs. By placing a predetermined value in the appropriate control register a port may be set up as an input or an output. The 6522 will actually allow the the programmer to define each individual port line as an input or an output. (The word 'programmer', incidentally, refers to the person who writes the machine operating system, so that the software configuration of the ports is usually permanent as far as the user is concerned). It is more usual, however, to use 8-bit ports as *all* inputs or *all* outputs. Figure 2 shows an example of how Port A can be programmed to act as an output by setting all bits in the Data Direction Register to 1. Here, the actual data content, or data value, sent to the port is 10101010 (AAH).

Some computers, for example the BBC Micro, have one or more ports available to the user enabling external devices to be controlled. The BBC Micro utilises two 6522 VIAs. The ports of one VIA are set up for the keyboard interface and hardware control, while those of the other function as the printer and user ports.

In the BBC Micro, the video signal for the monitor is provided by two VLSI devices; a 6845 Cathode Ray Tube Controller (CRTC), and a customised video processing chip (SC094) which is a ULA (Uncommitted Logic Array) device produced specifically for the BBC Micro.

In the Tatung Einstein microcomputer, a Z80-based machine, the video output is provided by a TMS 9129 VDP (ViDeo Processor) chip which is under the control of the Z80 MPU. The display memory (screen RAM) is provided by two 16K × 4-bit dynamic RAMs (DRAMs). Figure 3 is a schematic representation of this arrangement. The Einstein keyboard is controlled by two ports contained within an AY-3-8910 Programmable Sound Generator (PSG) device. These two ports are general-purpose programmable types and are shown in Figure 4.

The Keyboard

A microcomputer keyboard enables system commands to be entered and displayed on the monitor screen, and also various pieces of software (e.g. utilities) to be called up and loaded into RAM. The keyboard is also required to 'boot up' the operating system by, for example, pressing CTRL and BREAK keys simultaneously.

The ASCII Character Set

The American Standard Code for the Interchange of Information (ASCII) is an international standard in computer equipment which dates back to early teleprinter and teletype equipment. The ASCII code is basically a 7-bit one, although 8 bits is the standard size of data words used in microcomputers. 2^7 bits provide a total of 128 different ASCII codes, but these are usually expressed as 8-bit values where the most significant bit is set to zero. In serial data transmission, the eighth bit (bit 7) can be used for parity, which is a method of detecting errors. There are two forms of parity checking; even (which checks for an even number of logic '1's in a byte) and odd (which looks for an odd number of logic '1's in a byte). The eighth bit could also be used for graphics codes, providing 128 additional characters (1000 0000 = 128), but this is not

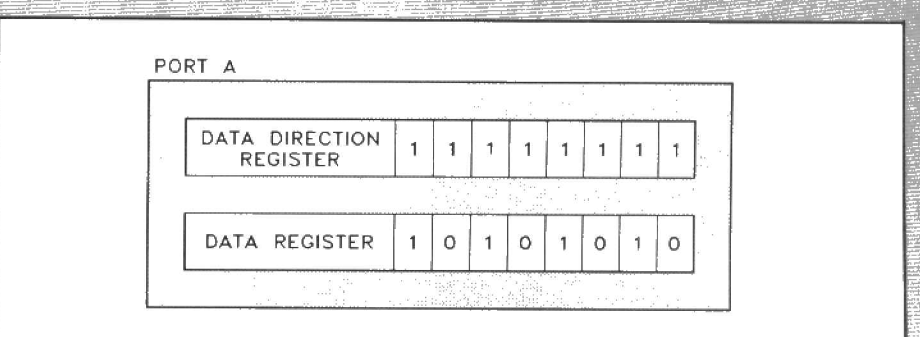


Figure 2. I/O port register contents.

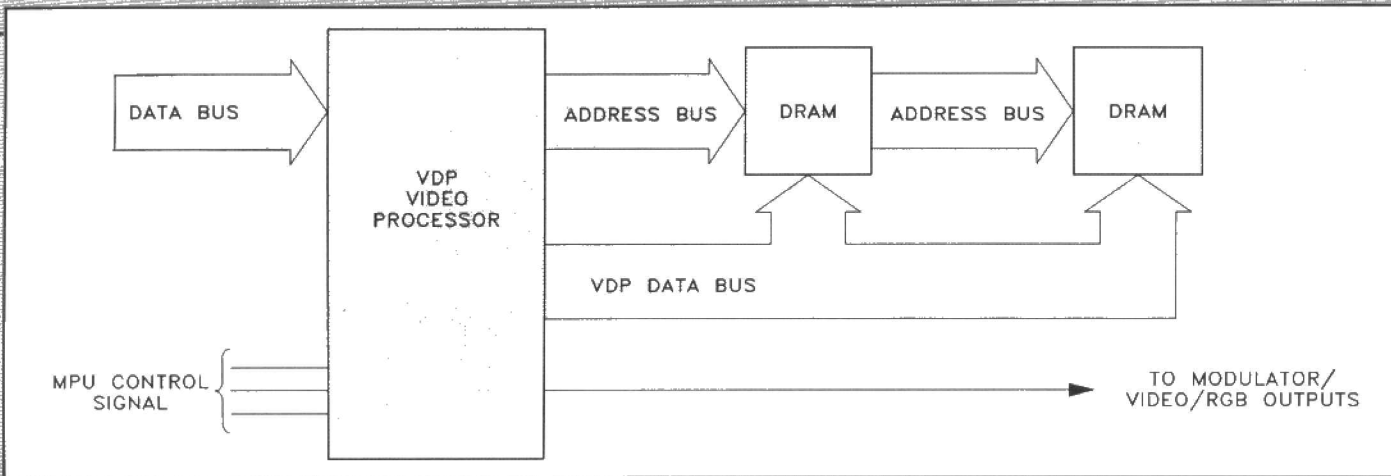


Figure 3. Einstein video interfacing circuit.

standard from one machine to another.

Figure 5 shows the standard ASCII character set, including the original names of the codes produced by using the CTRL key. 07H, for example, is the hex code for BEL which would sound a real bell on a teletype. Nowadays, 07H is used to generate a 'bleep' sound. Referring again to Figure 5, 'g' in the right-hand column has been assigned the hex code 67H (0110 0111 in binary). Pressing the SHIFT and 'G' keys simultaneously will produce 47H (0100 0111 in binary) which represents upper case 'G'. The SHIFT key, therefore, alters the logic level of bit 5. Similarly, holding down CTRL while pressing 'G' will give 07H (0000 0111 in binary), which represents the BEL code mentioned earlier. This code is the same as for 'G', except that this time bit 6 is changed.

Keyboard Operation

Keyboard operation is much more difficult to observe than one would perhaps expect, particularly in a situation where only a 2-channel oscilloscope is available. A logic analyser (to be covered in Part 4) would be very useful for observing the contents of the interface chip data lines.

The keyboard consists of a matrix of push-to-make switches, and is an input device which sends 8-bit binary codes along the data bus to the MPU. The diagram in Figure 7 shows a typical (8 × 8) matrix arrangement where each side of the matrix is connected to an 8-bit port (The SHIFT and CTRL keys are not part of the matrix, but are wired as shown in Figure 6). These ports are provided by a VLSI device, such as the AY-3-8910 PSG, or another device which is in, or compatible with, the same family as the MPU being used. For example, 6500 and 6800 series VLSI devices are largely compatible. Keyboard units, such as those used with IBM-compatible PCs, may have their own built-in logic in the form of a VLSI chip known as a keyboard controller. This is normally a single-chip microcontroller, but despite the increased complexity the principle of operation is similar to the above. Other methods of keyboard encoding use, for example, 74145 decoder drivers and 74251 data selectors in conjunction with a VLSI interface device. A keyboard may also be operated on an interrupt-driven basis.

The I/O ports are set up by the MOS

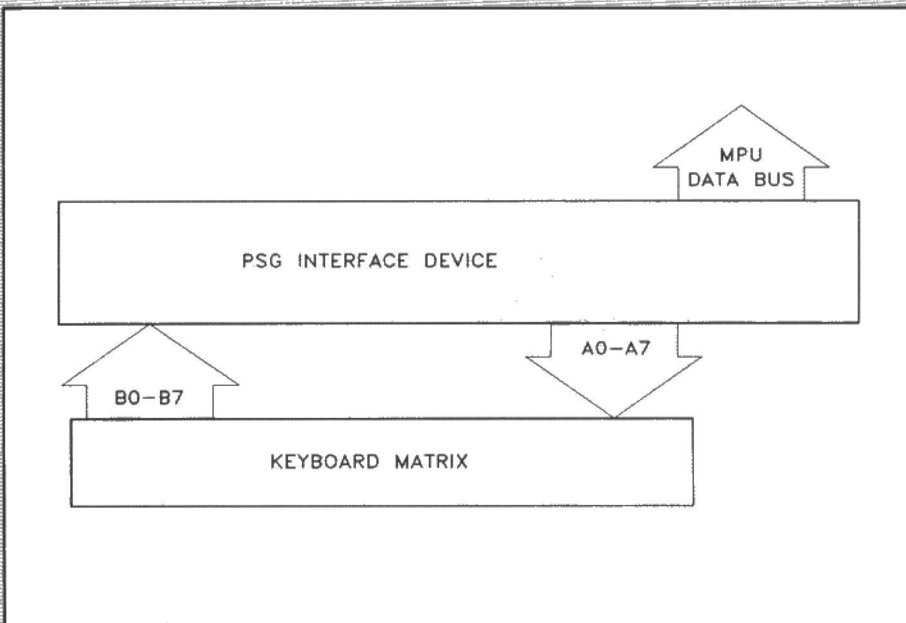


Figure 4. Einstein keyboard interface.

CODE	CHAR	CODE	CHAR	CODE	CHAR	CODE	CHAR
00	NUL	20	space	40	@	60	'
01	SOH	21	!	41	A	61	a
02	STX	22	"	42	B	62	b
03	ETX	23	£	43	C	63	c
04	EOT	24	$	44	D	64	d
05	ENQ	25	%	45	E	65	e
06	ACK	26	&	46	F	66	f
07	BEL	27	'	47	G	67	g
08	BS	28	(	48	H	68	h
09	TAB	29	)	49	I	69	i
0A	LF	2A	*	4A	J	6A	j
0B	VT	2B	+	4B	K	6B	k
0C	FF	2C	,	4C	L	6C	l
0D	CR	2D	-	4D	M	6D	m
0E	SO	2E	.	4E	N	6E	n
0F	SI	2F	/	4F	O	6F	o
10	DLE	30	0	50	P	70	p
11	DC1	31	1	51	Q	71	q
12	DC2	32	2	52	R	72	r
13	DC3	33	3	53	S	73	s
14	DC4	34	4	54	T	74	t
15	NAK	35	5	55	U	75	u
16	SYN	36	6	56	V	76	v
17	ETB	37	7	57	W	77	w
18	CAN	38	8	58	X	78	x
19	EM	39	9	59	Y	79	y
1A	SUB	3A	:	5A	Z	7A	z
1B	ESC	3B	;	5B	[	7B	{
1C	FS	3C	<	5C		7C	|
1D	GS	3D	=	5D	]	7D	}
1E	RS	3E	>	5E	↑	7E	~
1F	US	3F	?	5F	←	7F	RUBOUT

Figure 5. ASCII character set.

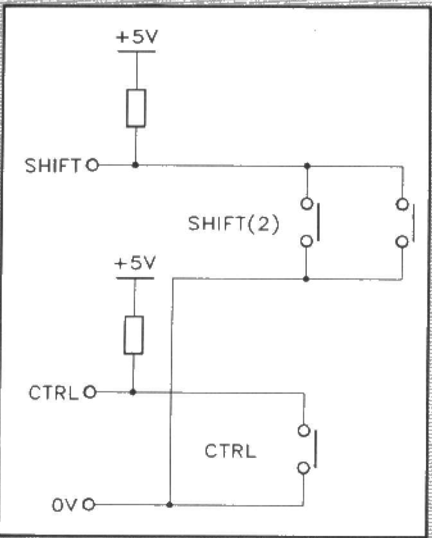


Figure 6. SHIFT and CTRL key connections.

software. In other words, an 8-bit port can be programmed as an input or an output port by placing a pre-determined value in the appropriate register of the interface device. The diagram in Figure 4 shows that lines 0 – 7 of Port A are set up as outputs, while lines 0 – 7 of Port B are set up as inputs.

As the port inputs have pull-up resistors of 13K, the input lines (B0 – B7) are normally held at logic 1. The output lines (A0 – A7) are set to logic 0 by the MOS. When a key within the matrix has been depressed, one of the input lines of the port is connected to an output line and is thus connected to logic zero. If a key is held down, then the MOS will scan the matrix to ascertain exactly which key has been pressed. The appropriate ASCII code for a specific character cannot be observed wholly on any one port. With reference to Figure 7, if the 'T' key is pressed then lines A3 and B5 of the matrix will be shorted together. The MOS, in conjunction with the design of the interface chip, determines which ASCII code is 'looked up' and then placed on the data bus of the device. Figure 8 is an ASCII conversion chart that cross-references the standard ASCII character set with the corresponding decimal, hexadecimal and 7-bit binary codes.

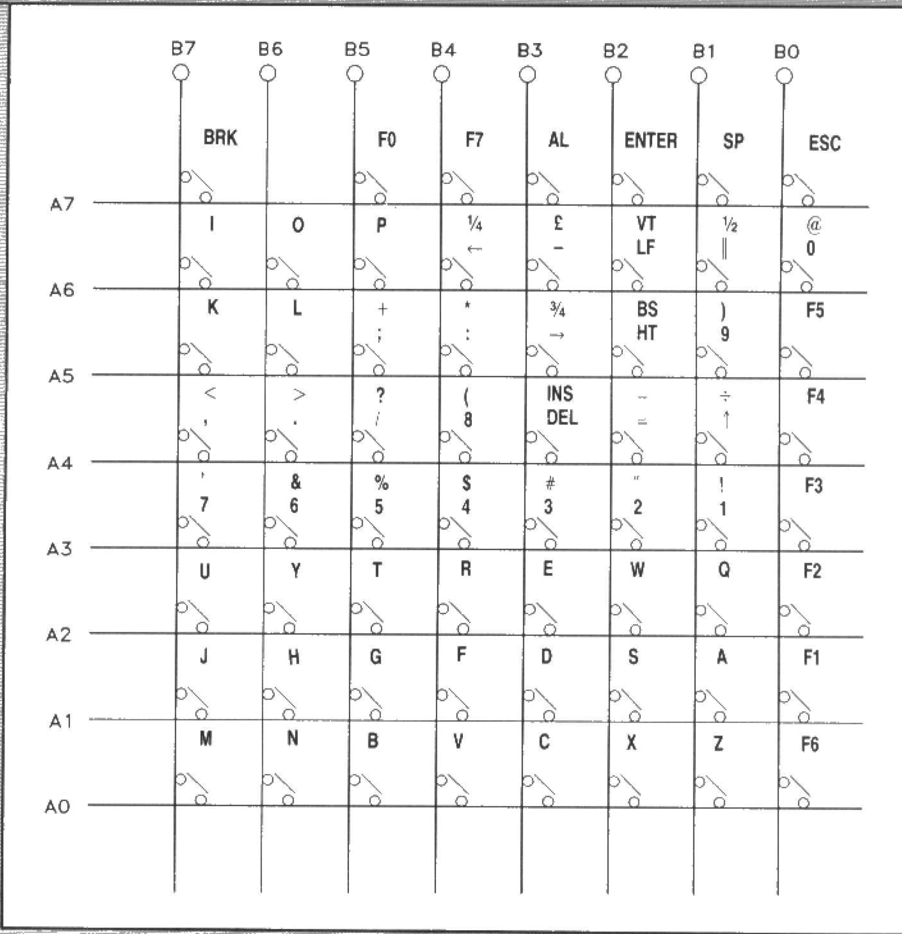


Figure 7. Keyboard matrix.

Char	Dec	Hex	Binary	Char	Dec	Hex	Binary	Char	Dec	Hex	Binary	Char	Dec	Hex	Binary
NUL	0	0	0000000	@	64	40	1000000	space	32	20	0100000	'	96	60	1100000
SOH	1	1	0000001	A	65	41	1000001	!	33	21	0100001	a	97	61	1100001
STX	2	2	0000010	B	66	42	1000010	"	34	22	0100010	b	98	62	1100010
ETX	3	3	0000011	C	67	43	1000011	£	35	23	0100011	c	99	63	1100011
EOT	4	4	0000100	D	68	44	1000100	$	36	24	0100100	d	100	64	1100100
ENQ	5	5	0000101	E	69	45	1000101	%	37	25	0100101	e	101	65	1100101
ACK	6	6	0000110	F	70	46	1000110	&	38	26	0100110	f	102	66	1100110
BEL	7	7	0000111	G	71	47	1000111	'	39	27	0100111	g	103	67	1100111
BS	8	8	0001000	H	72	48	1001000	(	40	28	0101000	h	104	68	1101000
TAB	9	9	0001001	I	73	49	1001001	)	41	29	0101001	i	105	69	1101001
LF	10	A	0001010	J	74	4A	1001010	*	42	2A	0101010	j	106	6A	1101010
VT	11	B	0001011	K	75	4B	1001011	+	43	2B	0101011	k	107	6B	1101011
FF	12	C	0001100	L	76	4C	1001100	,	44	2C	0101100	l	108	6C	1101100
CR	13	D	0001101	M	77	4D	1001101	-	45	2D	0101101	m	109	6D	1101101
SO	14	E	0001110	N	78	4E	1001110	.	46	2E	0101110	n	110	6E	1101110
SI	15	F	0001111	O	79	4F	1001111	/	47	2F	0101111	o	111	6F	1101111
DLE	16	10	0010000	P	80	50	1010000	0	48	30	0110000	p	112	70	1110000
DC1	17	11	0010001	Q	81	51	1010001	1	49	31	0110001	q	113	71	1110001
DC2	18	12	0010010	R	82	52	1010010	2	50	32	0110010	r	114	72	1110010
DC3	19	13	0010011	S	83	53	1010011	3	51	33	0110011	s	115	73	1110011
DC4	20	14	0010100	T	84	54	1010100	4	52	34	0110100	t	116	74	1110100
NAK	21	15	0010101	U	85	55	1010101	5	53	35	0110101	u	117	75	1110101
SYN	22	16	0010110	V	86	56	1010110	6	54	36	0110110	v	118	76	1110110
ETB	23	17	0010111	W	87	57	1010111	7	55	37	0110111	w	119	77	1110111
CAN	24	18	0011000	X	88	58	1011000	8	56	38	0111000	x	120	78	1111000
EM	25	19	0011001	Y	89	59	1011001	9	57	39	0111001	y	121	79	1111001
SUB	26	1A	0011010	Z	90	5A	1011010	:	58	3A	0111010	z	122	7A	1111010
ESC	27	1B	0011011	[	91	5B	1011011	;	59	3B	0111011	{	123	7B	1111011
FS	28	1C	0011100		92	5C	1011100	<	60	3C	0111100	¦	124	7C	1111100
GS	29	1D	0011101	]	93	5D	1011101	=	61	3D	0111101	}	125	7D	1111101
RS	30	1E	0011110	↑	94	5E	1011110	>	62	3E	0111110	~	126	7E	1111110
US	31	1F	0011111	←	95	5F	1011111	?	63	3F	0111111	RUBOUT	127	7F	1111111

Figure 8. ASCII conversion chart.

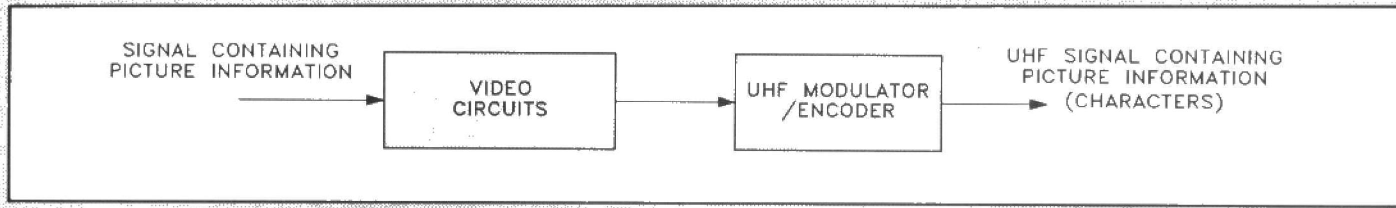


Figure 9. Output from microcomputer to monitor.

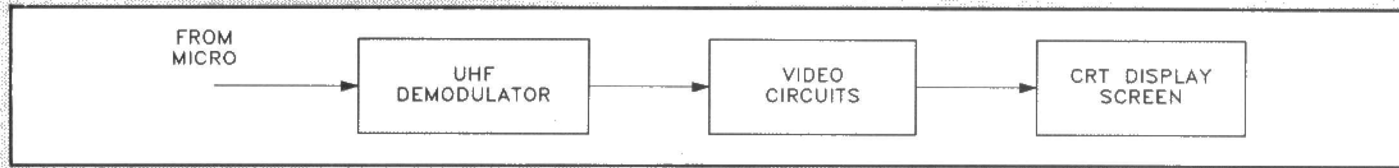


Figure 10. Input to monitor from microcomputer.

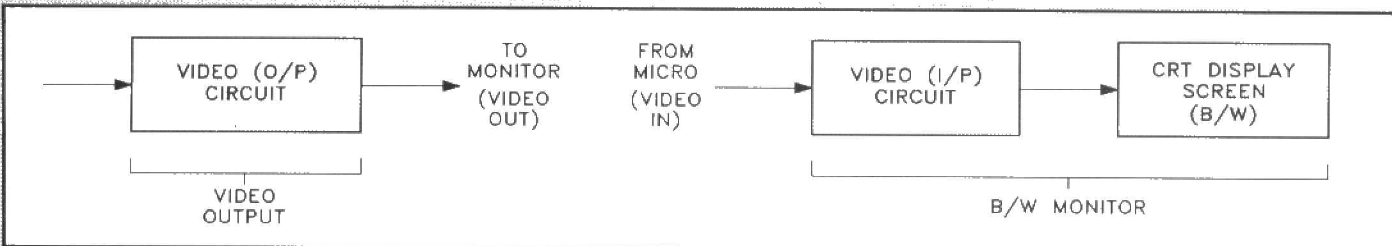


Figure 11. Direct connection to a video monitor (B/W).

The Video Monitor

The VDU, or monitor, is the piece of hardware which enables most program activity and results to be observed on a screen. It is usually a physically separate item, containing the cathode ray tube (CRT), associated drive electronics and power supply. Each picture 'frame' of the average home computer video display is made up of around 600 lines, along each of which the brightness varies (producing the 'dots', or 'pixels' (picture elements), of each character), and 25 of these frames are shown on the screen every second. In this article we will be dealing with a monochrome (black and white) monitor for simplicity, as colour monitors are much more complex. However, the principles used will help the technician to approach colour monitor operation and faults. Please do not confuse the term 'monitor' with 'monitor program' (which refers to a type of operating system).

Confusion can sometimes arise when dealing with monitors, and so some clarification would be useful at this stage. A home computer, for example, can have more than one video output. In the case of the BBC Micro, three such outputs are available:

(1) UHF
(2) VIDEO
(3) RGB

It is essential that each type of output is understood by the technician, particularly if the making up of computer-to-monitor connecting leads is anticipated.

The UHF output is normally a phono socket, rather than the standard coaxial socket found on television sets. As its name suggests, this output signal is in the form of a ultra high frequency television-type signal exactly suited for use with a domestic UHF TV receiver. This system is used mainly with home computers for this reason, so that a special purpose monitor is not required. The output signal has the same composition as a TV broadcast signal, and colour computers fitted with a UHF output normally include colour-encoding circuits so that a colour TV set will produce a full colour display. Figure 9 shows, very simply, the relevant output stages of the microcomputer.

A microcomputer with a UHF output contains a device known as a UHF modulator. This is an oscillator circuit providing a UHF carrier frequency, which is then modulated with the signals required to drive the video and synchronisation ('sync') circuits of the TV set (and in the case of some home computers, the sound channel as well). It must be remembered that although the computer video signal is digitally derived, it is converted (via the modulator) to the analogue form required by the TV set. The TV set will demodulate the computer signal as if it were a normal TV programme, providing the 'digital' picture information and the video signals which drive the CRT. Figure 10 shows a block diagram of the TV set while it is being used as a monitor.

The UHF modulator circuit within a microcomputer is easily recognised as a self-contained unit inside a rectangular screening can. It is also the last stage before the UHF output socket. Another socket on most microcomputers is the 'Video' socket, which provides the video and sync information (known as 'composite video') from a stage just prior to the UHF modulator. This can be fed directly to a conventional monitor, or to a TV set with a composite video input (e.g SCART/Peritel socket). The UHF modulation and demodulator stages are bypassed, and this results in a better picture with improved resolution. Figure 11 shows the direct connection made from a video output stage to the standard video input socket of a video monitor. Please note that a micro without a conventional video output cannot be used with a standard video monitor. Likewise, a computer without a video output socket cannot be used with a conventional TV set. Attempts to do so should not be made!

The video output socket in a microcomputer provides a standard composite video signal with a specified amplitude of 1V Pk-to-Pk. A simplified waveform diagram of this signal is shown in Figure 12. The period of this waveform (64·125μS) corresponds to the line synchronisation frequency of the signal i.e. 15·625kHz.

RGB (pronounced 'arr-gee-bee') is an acronym for Red-Green-Blue, these being the primary colours that form a television picture, and from which all others can be derived. The RGB signal is different again as unlike the video signal it is not composite – separate channels are required for the red, blue, green and video/sync components of the display. The first three separate channels drive the guns of the tube directly, while the fourth sync component references the monitor's timebases. Figure 13 illustrates this, although for simplicity the sync channel is not shown.

The RGB system gives the best results with a colour display simply because many stages have been eliminated. The average home computer with colour graphics will normally have a RGB output for direct connection to a monitor, and usually a colour signal at its UHF output as well. If the RGB monitor and TV display were to be compared, it would be found that the monitor display was much better.

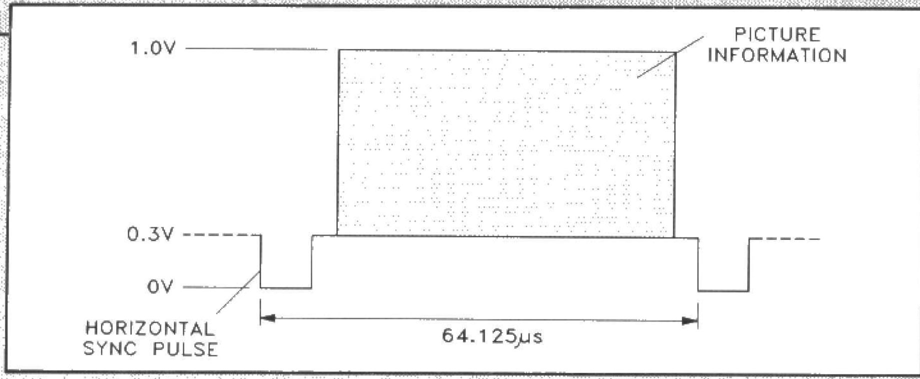


Figure 12. Video waveform (one complete picture line).

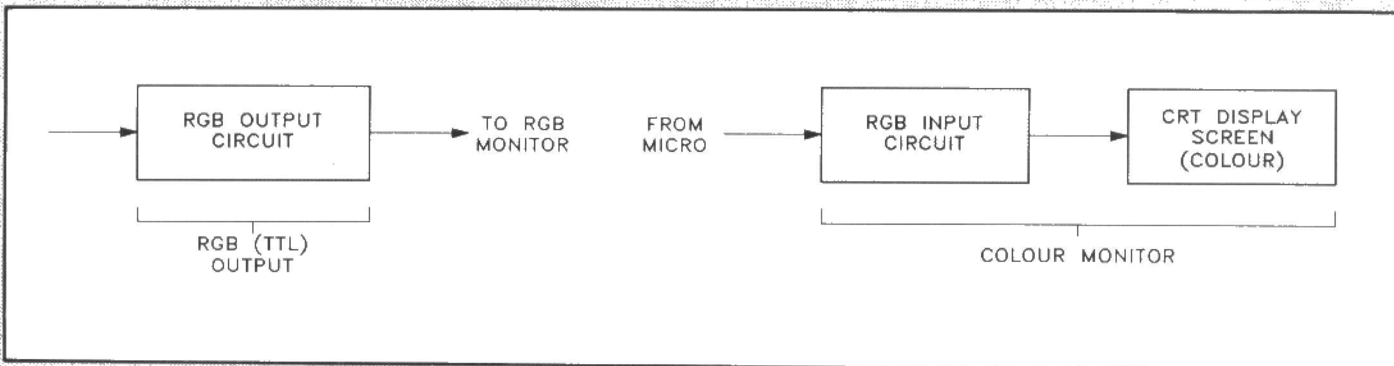


Figure 13. Direct connection to an RGB (colour) monitor.

To offer a colour display through the UHF output, the computer has to encode the separate R, G, B, video and sync information to the broadcast colour standard (which in the UK is a system known as PAL). Such a process results in a colour composite video signal similar in composition to that of a normal off-air TV or VCR programme. This signal is then passed to the UHF modulator and is processed in the same way as mentioned earlier. At the TV end, the UHF signal is demodulated and the composite video signal decoded, reconstituting the information required to drive each of the three tube guns and the set's timebases. All of this circuitry is bypassed with the RGB system, resulting in a much more readable picture with less 'dot crawl' (introduced by the PAL process) and superior resolution. This is why RGB monitors are always recommended for prolonged or serious use.

Some Practical Investigation

Working on microcomputers usually means dealing with low DC voltages of about 5V DC, and possibly up to 20V DC. All such equipment (unless portable) is powered by the mains and therefore the technician will have to deal with mains power supplies. In addition, the EHT voltages present in monitors are even higher; voltages of around 10kV are present in monochrome monitors while colour monitors harbour potentially lethal potentials of around 20 to 30kV. The differences between the two are academic because both can be harmful, just like mains voltages. These high voltages are a necessary evil of microcomputer operation but they need not present any danger to the individual if the usual precautions are taken. It is always good practice not to remove cases or covers of any item while it is still switched on or plugged into the mains. Remember that a moment's thoughtlessness or laziness could result in severe damage being caused to the equipment – or technician. Isolation from power supplies is also important when attaching test probes from a meter or scope to the unit being serviced. Accidental short circuits caused while the unit is powered up during servicing could introduce faults additional to those already being investigated. Finally, one must never have both hands within a piece of equipment with mains or EHT voltages still present. Should a circuit be completed through an individual's arms, then current would pass through the heart, possibly proving fatal. If work has to be undertaken on live mains equipment, then it must be supplied with power via a mains isolating transformer.

Memory Devices

Although this article deals primarily with I/O circuits and systems, it is appropriate to mention memory devices, having already mentioned screen RAM and registers in peripheral control devices, which can be thought of as memory locations (in the case of the BBC Micro (6502), these registers are treated as memory-mapped locations).

In the Einstein, the main (MPU) memory is provided by eight 64K × 1-bit DRAMs, which give a total of 64K bytes of memory. 64K is the maximum amount of memory that an 8-bit MPU such as the Z80 (or 6502) can address, and therefore additional memory such as the screen RAM (16K) and ROM devices are considered to outside of the 64K memory map. The BBC Micro has a maximum memory capacity of 32K RAM and 32K ROM. Additional ROM chips, such as wordprocessors and PASCAL interpreters, are switched in (or 'paged') instead of the BASIC ROM.

Memory chips are 'organised' in bit sizes. In other words, a RAM chip such as the 2114 4K static RAM (SRAM) is organised as 1024 × 4-bit words (also known as 'nibbles' or half-bytes). Figure 14 shows the pin-out connections of the 2114 package. It can be seen that there are 10 address lines (A0 – A9, corresponding to the (2^{10} =) 1024 words to be addressed), and 4 data lines for the 4 data bits.

Please note that the 4K value refers to 4K *bits* and not 4K bytes. To achieve 1K byte, 2 × 2114 chips would be required. In this case, the address pins of both ICs would be wired in parallel to provide a total of 1K × 8 bits. The way in which memory ICs are connected together, or configured, determines the use which they are put. Figure 15 shows how the 2114 RAMs are connected.

Individual memory chips are the 'building blocks' of any memory array. The 4164 DRAM chip used in the Einstein is organised as 64K × 1-bit cells, and thus the 8 such chips found in the computer provide (64 × 1 × 8 =) 64K bytes of RAM. A 4416 RAM provides 16K × 4-bit cells, and so two chips suitably organised will provide (16K × 4 × 2 =) 16K bytes. Such an arrangement is used in the Einstein's screen memory. The Einstein ROM makes use of a 2764 chip, which is a 8K × 8-bit device. Each of these, therefore, has a 8K byte capacity.

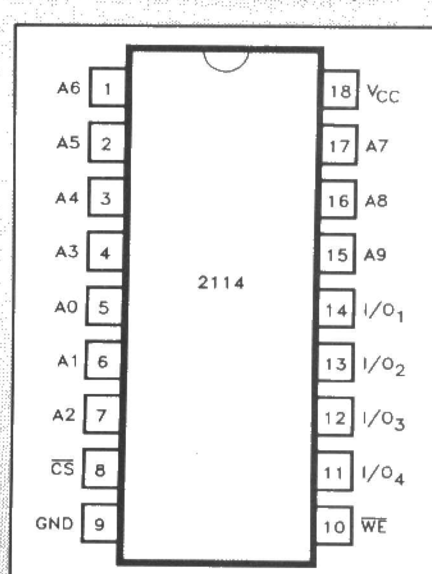


Figure 14. 2114 4K RAM pin connections.

Continued on page 68.

Design and Application of SEQUENTIAL LOGIC

PART ONE

by Graham Dixey
C.Eng.,M.I.E.E.

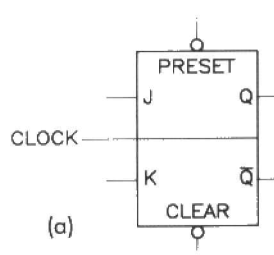
Introduction

There are two classes of digital logic, known as 'combinational logic' and 'sequential logic'. The former uses gate arrays to obtain predictable responses to all possible input combinations. Sequential logic, on the other hand, makes use of flip-flops either to generate or 'process' specific time-dependent, binary patterns when excited by a repetitive input, such as a train of pulses. The latter logic type may be broadly subdivided into 'counters' and 'registers'. From the point of view of 'seeing digital circuits at work', so to speak, sequential logic offers the experimenter a great deal of scope in exploring this fascinating facet of electronics. There are many circuits to investigate and, apart from the occasional use of an oscilloscope, the required test gear is not expensive. The intention of this series is to show how a wide range of reliably working circuits can be designed, using the most suitable technology for each particular case – or, where two or more choices exist, to develop both and hence draw a comparison between methods and results.

The design of sequential logic circuits will make use of currently available integrated circuits, with little dependence upon discrete components except for the mundane, though vital, tasks of decoupling, providing pull-up loads, etc. Although even here there are two separate approaches. It is possible to design any sequential circuit by interconnecting flip-flops, perhaps with some extra gating. Commonly two flip-flops exist on a single IC, so that the design of an 8-stage counter, for example, would require the use of four ICs to provide the flip-flops alone. In many cases this approach is unnecessary; single counter and shift register packages exist which include all of the required flip-flops and gating. Some degree of flexibility is conferred upon such packages by the ability to 'hard wire' certain pins to specific potentials.

This is not to say that that which might be called the 'semi-discrete' approach is totally redundant. Manufacturers cannot be expected to provide for every possible requirement. There is a design approach to sequential circuits of this type that allows counters to be produced with absolutely any sequence, no matter how bizarre. This will be discussed in depth as well as those circuits which make use of the more complex IC packages.

It may be considered rather superfluous to say that counters and registers exist for some specific function rather than their own sake. Nonetheless, too often in text books the counter design culminates in the bare circuit. No attempt is made to show how such a circuit might be applied in practice, how in such applications the output has to be decoded, buffered, or otherwise modified to 'interface' the circuit with the device that it is intended to drive. Similarly, the presence of the clock pulse shown in such instances is often taken for granted without recourse to any discussion as to how it might be generated or to its desired attributes. In an attempt to balance the books somewhat, this series will 'reach the parts that other series have not reached' and show not just how to design the counter or register itself, but how to make it perform some of the many useful and interesting functions of which it is capable.



(a)

J	K	Qn	Qn+1	COMMENTS
0	0	0	0	NO CHANGE
0	0	1	1	
0	1	0	0	RESET
0	1	1	0	
1	0	0	1	SET
1	0	1	1	
1	1	0	1	TOGGLE
1	1	1	0	

(b)

J	K	Qn	Qn+1
0	0	X	Qn
0	1	X	0
1	0	X	1
1	1	X	$\bar{Q}$n

(c)

Figure 1. (a) Circuit symbol, (b) full truth table for a JK flip-flop and (c) the same truth table simplified by using 'don't cares'.

A Choice of Technology – TTL or CMOS

For many years now the designer of logic circuits has had available two extensive IC families, known as the 7400 series and the 4000 series; the former uses TTL techniques, based on bipolar transistors; the latter makes use of complementary MOS devices (CMOS). The situation is now changing with the introduction of new ranges under the '74 series banner'. These bear the distinguishing letters HC (High speed CMOS), as in 74HC00, and AC for Advanced High speed CMOS. They offer pin for pin compatibility with the older ranges and are to be preferred in new designs. As far as this series is concerned, their relative merits will be discussed where applicable. But it should be borne in mind they that do not change the essential principles of design except inasmuch that power consumption, speed, etc., are influenced by such choices. In general, a complete circuit design using either standard TTL or LSTTL chips will still work with HC devices since the operating speed of the latter will permit this.

The Flip-Flop: the Basic Building Block

This is the starting point then – an examination of the smallest valid element. There will be no consideration here of flip-flops wired up from the logic gates themselves. A microscopic examination of the silicon chip itself would reveal that this is how such devices are structured, but it is unnecessary to delve this far. Simple flip-flops *can* be made up from gate packages but, except in rare instances, such devices are of little real use. We are left with two devices only – the JK flip-flop and the D flip-flop. Either can be used in the design of both counters and registers. In general, though, JK flip-flops are used in counters and D types in registers. So, as we are going to discuss counters first of all, the JK will be the basic building block we shall use. We must be fully familiar with it. First, the circuit symbol of Figure 1(a).

This symbol shows a box with three input connections and two outputs. At the

top and bottom are two further connections, an obvious difference between these and the others being the small 'bubble' where they enter the package outline. Two of the inputs are marked J and K and are known as the 'steering inputs'; the third is the clock, which is used to initiate the required events. The outputs are called Q and $\overline{Q}$ (Q-bar or NOT Q), and are said to be complementary since when one is at logic 0 the other is at logic 1 and vice-versa. Either of these outputs may be used in particular cases but Q is usually considered as being the principle output. When we say that a flip-flop is 'storing' a binary digit, we are referring to the state of the Q output.

Preset and Preclear

Before we can discuss these terms it is necessary to define the terms SET and RESET (also called clear). These are opposite states of the flip-flop – being a binary device it can only have the two states. They are defined as follows:

When Q = 0, the flip-flop is RESET.
When Q = 1, the flip-flop is SET.

Thus, when we talk about the operation of SETTING the flip-flop we mean causing the Q output to go to logic 1 and, when we refer to RESETTING or CLEARING the flip-flop, we mean causing the output to go to logic 0. There are two ways in which the Q output of a JK flip-flop can be set or reset. One way is to preset the logic levels at the J and K inputs to certain values; the arrival of a clock pulse after this setting-up operation will cause the required action to occur. This method will be discussed in more detail shortly. It is obvious that it is dependent upon a clock pulse being applied – for this reason it is said to be 'synchronous'.

The other method is independent of the clock (and, hence, is termed 'asynchronous'). All one has to do is to take either the 'preset' or 'preclear' pin momentarily to logic 0 for the flip-flop to be set or cleared respectively. The round 'bubble', mentioned earlier, against each of these inputs signifies this fact. The preset and preclear connections are then said to be 'active low' or 'negative acting'. The main use for these connections is for setting up a 'reset line' for a complete counter or register, or when presetting data into one of these devices (Figure 2).

Truth Table for the JK Flip-Flop

The truth table is a straightforward and effective way of showing how the flip-flop will behave in response to being clocked, for each of the four possible logical combinations that the steering inputs, J and K, can assume. This table is shown in Figure 1(b) and is seen to have eight lines, two being assigned for each JK combination. The logical value at the Q output, prior to clock, can obviously be either a 'zero' or a 'one' – hence the reason for using two lines.

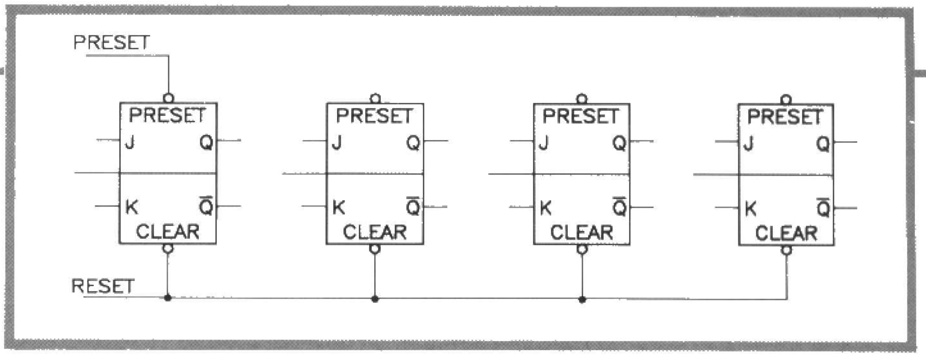


Figure 2. Setting up a reset line or a preset facility.

The columns Q_n and Q_{n+1} mean, respectively, the value of Q *before* the clock pulse, and the value of Q *after* the clock pulse. When this is understood the truth table is easy to interpret. In plain language the meaning of each pair of lines is as follows.

The first two lines (J = 0, K = 0) mean 'whatever the initial value of Q, after the clock pulse it will be unchanged'; in the *comments* column it is noted that this is the *no change* state.

The next two lines (J = 0, K = 1) mean 'whatever the initial value of Q, after the clock pulse it will be logic 0'. In the *comments* column we see that this is the SET state.

The next two lines (J = 1, K = 0) mean 'whatever the initial value of Q, after the clock pulse it will be logic 1'. In the *comments* column we see that this is the SET state.

In the final two lines (J = 1, K = 1) the meaning is that 'whatever the initial value of Q, after the clock pulse it will be the opposite'. This is known as the *toggle* mode. This latter mode is of particular importance, as we shall soon see.

It will be noted that in describing the above, the phrase 'whatever the initial value of Q, ...' occurred in each case. This leads to a shorthand way of writing down the above truth table and is, by the way, also useful in other situations as well. The secret is to refer to cases, such as the above where the initial value of Q is not important, as 'don't cares'. A don't care condition is designated by an 'X'. Figure 1(c) shows the truth table of Figure 1(b) simplified by using this convention. There are now only four lines doing the job of the original eight.

In order to use the features described by the above truth table, a clock pulse is required. This should meet certain criteria if reliable operation is to be achieved.

The Clock and Set/Reset Pulses

The minimum length of these pulses is determined by the time that it takes for the flip-flop to change state. For standard TTL devices this is about 25 nanoseconds. However, low power TTL may require longer clock and set/reset pulses, of the order of 200 and 100 nanoseconds, respectively. Conversely, high power logic gives faster switching speeds with pulse widths as short as 10 nanoseconds being possible. Rise and fall times for the pulses are less critical, up to 5 microseconds being permissible. Figure 3 shows a single clock pulse which is defined by some of the terminology that will be met as we progress.

The Master-Slave Flip-Flop, Level and Edge-Triggering

Descriptions of flip-flops in catalogues or data books will often include reference to these terms. It is worth spending a little time explaining what they mean.

Taking the term 'master-slave' flip-flop first. Many JK flip-flops are of this type. The internal structure consists of two simpler flip-flops in series, the first being driven directly from the clock pulses, the second from the same clock source but inverted (see Figure 4). It is a characteristic of both of these internal flip-flops that they will change state on the 'positive edge' (see Figure 3) of the clock pulse. Thus, the first flip-flop (the master) changes state as soon as the clock pulse is received. The slave does nothing at this time because the inverter in the clock line means that it will be clocked with a 'negative edge'. The Q and $\overline{Q}$ outputs of the master provide the steering inputs to the slave; they are such

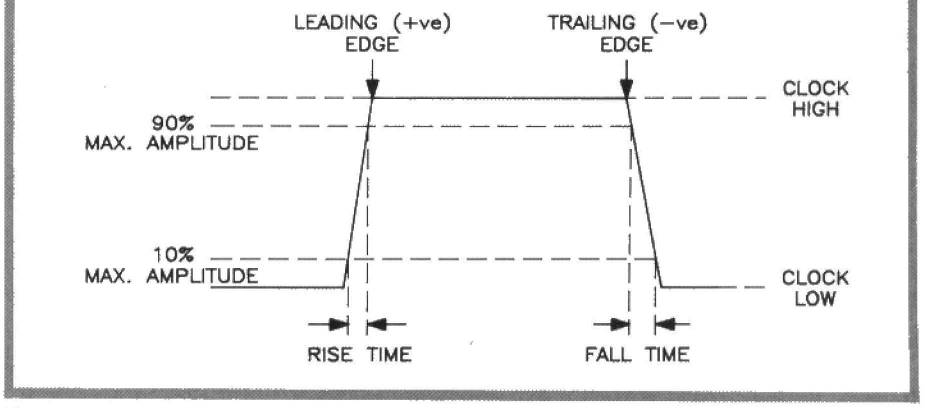


Figure 3. The clock pulse.

that they will force the slave to change state when it gets a positive clock edge. This will be forthcoming as soon as the clock pulse goes low, because then the inverted clock pulse will, of course, go high. The slave flip-flop immediately changes state, its Q output becomes either set or reset, as required, and this is the final Q output of the JK flip-flop.

It should be evident from the above description that such flip-flops are 'level sensitive', meaning that it is the actual 'logic level' itself that produces the change of state.

Contrast this with the 'edge triggered' device. This changes state during the 'transition' between logic levels. For example, a flip-flop may be described as being 'positive edge clocked', meaning that the change of state occurs *during* that short period when the clock pulse is rising from logic 0 to logic 1! Both of these ideas are shown in Figures 5(a) and 5(b). These give a clue to the reason why one method may sometimes be preferred over the other.

From Figure 5(a) we see that there is a relatively long time between the positive and negative clock edges. Suppose that at the beginning of the clock period $J = 1$ and $K = 0$. These steering inputs set up the conditions for the flip-flop to go the SET state when the clock pulse goes low, at the negative clock edge. As we may remember, because of the master-slave action, the master has already 'set itself' (it did so at the clock pulse leading edge); it is merely waiting for the negative edge to arrive so as to pass this state on to the slave. But now suppose that before the negative edge arrives the state of J and K inadvertently reverse so that $J = 0$ and $K =$

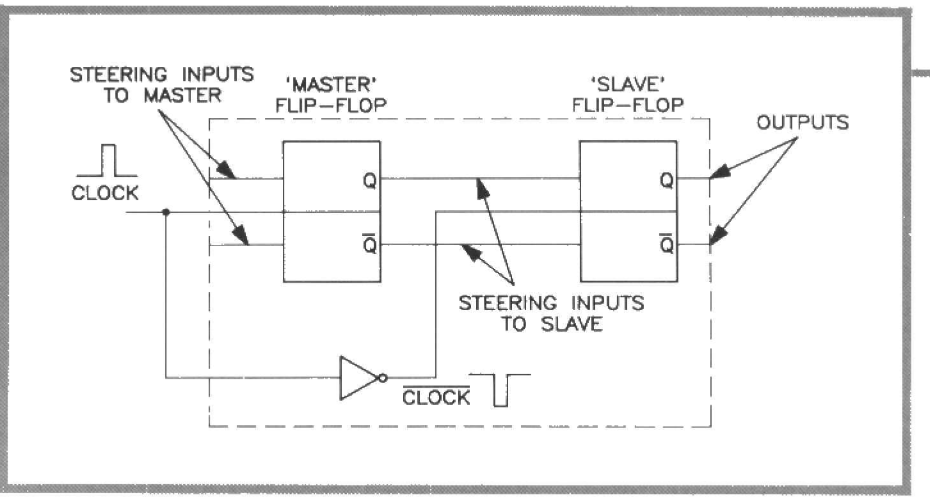


Figure 4. The master-slave flip-flop.

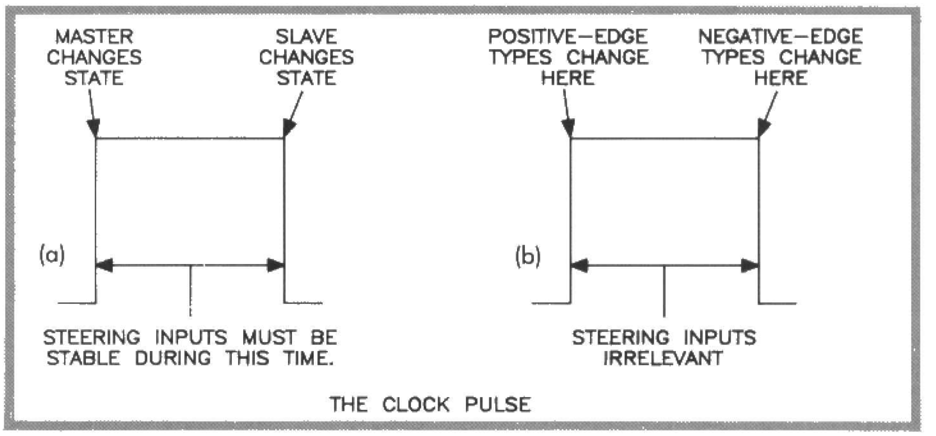


Figure 5. Showing (a) level triggering and (b) edge triggering of flip-flops.

1. The master flip-flop immediately resets, so changing the steering inputs to the slave. If nothing else happens before the negative edge of the clock pulse arrives, the end result will be that the final Q output of the JK flip-flop will be reset when it should have been set. This is essentially a timing problem because of the delay between the two events – the arrival of the positive and negative clock edges.

Figure 5(b) shows the same clock pulse, but with an essential difference – not in the pulse itself, but in the way the flip-flop reacts to it. The change in Q is instantaneous. D flip-flops are often of this type.

There is a simple rule. If there is any likelihood that the logic levels applied to J and K may vary during the duration of the clock period, then edge-triggered flip-flops should be used. Otherwise, if the stability of J and K during these periods can be guaranteed, then level-triggered flip-flops will be adequate.

The JK Flip-Flop as a Binary Divider

Two points regarding the behaviour of the JK flip-flop when it is clocked are now worth noting.

(i) When the flip-flop is in the 'toggle mode', with both J and K inputs wired to logic 1, a change of state occurs for every clock pulse.

(ii) This change of state only occurs when the clock input goes from logic 1 down to logic 0.

This means that, while a complete clock pulse includes *two* level transitions – one at the positive edge that has no apparent effect, the second at the negative edge that produces the final change of state – the change of state itself consists of just *one* level transition (Figure 6). This may be from logic 0 to logic 1 (when the flip-flop is being set) or from logic 1 to logic

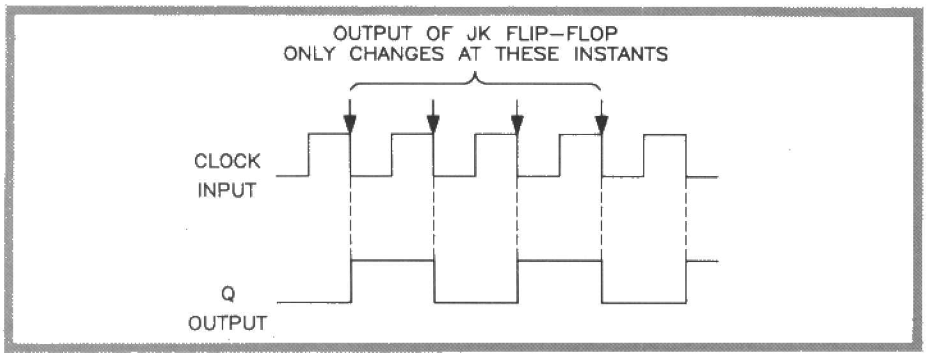


Figure 6. The JK flip-flop binarily divides the clock frequency.

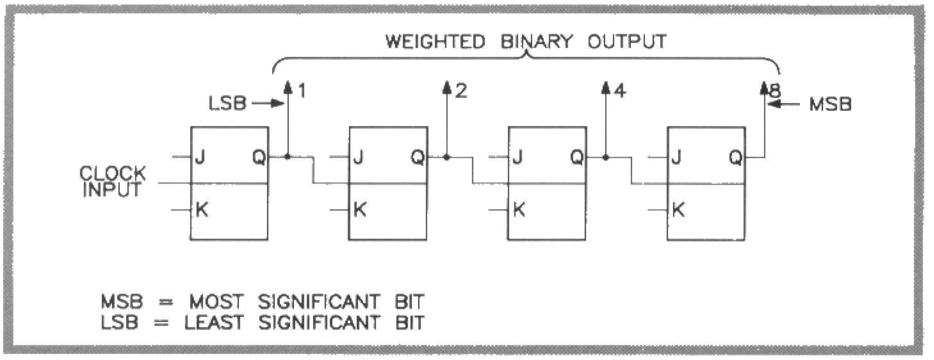


Figure 7. A 'modulo-16' 8421 weighted pure binary counter schematic.

0 (when the flip-flop is being reset). A moment's thought will produce the conclusion that, if two transitions at the clock input produce only one transition at the output, then the input frequency is being divided into two! Thus, if each stage of a binary counter produces this binary division, then *two* stages will divide by four, three stages will divide by eight, four stages will divide by sixteen, and so on.

Counters that have these particular division ratios, 2, 4, 8, 16, etc., are termed 'pure binary counters'. There are ways of changing the ratios at will as we shall see.

Modulo and Weighting of a Counter

Counters are said to have a 'scale' or 'modulo'. These are just alternative terms for the number of individual states of the counter, which is the same thing as the division ratio just discussed. Thus a counter that divides the input frequency by eight may be variously described as 'a scale of eight counter', a 'modulo-8 counter' or as a 'divide-by-eight' counter.

Some counters are described as being 'weighted'. This means that each of the flip-flops can be considered as representing the column of a binary number; the numerical value of that column is called its 'weighting'. In the simple case of a four-stage pure binary counter, represented schematically in Figure 7, the weighting is 8421, derived by reading from MSB to LSB, that is of course from right to left. The addition of these digits, $8 + 4 + 2 + 1 = 15$, which in binary is 1111, clearly the maximum state of the counter. The total number of states is 16 since 0000 is also a state.

Power Supplies for TTL Circuits

Assuming for the moment that TTL is the logic being considered, the power supply must be good enough for the task. It should be well regulated, with an output that is held to $+5V \pm 0{\cdot}25V$. Where it is connected to the circuit board it should be decoupled with a $10\mu F$ tantalum electrolytic capacitor. Where it is connected to a chip it should be decoupled with a 100nF short-lead disc ceramic capacitor. In fact, it is usually sufficient to decouple every two TTL packages but, whereas you can have insufficient decoupling capacitors, you cannot have too many.

Manual Reset and Set Controls

As we have seen, the flip-flop can be preset or pre-cleared by pulsing the appropriate package pin low. This pulse may be generated in various ways, but an obvious and often practical method is to use a push-button that momentarily grounds the pin, as shown in Figure 8. Under these circumstances, a 'pull up' resistor should be wired between the pin and the $\pm 5V$ supply; a value of 330Ω is suitable. This should ensure a rapid rise time; a slowly rising reset voltage can produce uncertainties.

Asynchronous and Synchronous Counters

Asynchronous counters are also referred to as 'ripple through' or simply 'ripple' counters. These more graphic terms describe the device better than the more technical one. Because any changes that should take place do so one stage after another, the effect of these changes is seen to ripple through the counter. This also emphasises that, in such a counter, allowance must be made for the ripple to reach the last stage before the next clock pulse is applied. This obviously limits the speed of the counter. There is another less obvious snag as well. This is illustrated by the 3-stage ripple counter of Figure 9.

Suppose that the counter is holding the count ABC = 011. This immediately highlights a particular problem in describing counter sequences – the letters used to designate the flip-flop positions have to be reversed to get the binary number the 'right way round'. This is, of course, because the least significant bit of the counter is on the left whereas for the number it appears to the right. Well, that's got that out of the way, so on with the discussion.

The number following ABC = 011 is, of course, 100. This means that ALL flip-flops have to change, one after the other, starting with flip-flop C. The sequence goes like this:

	A	B	C	
Present state →	0	1	1	
Second state →	0	1	0	(flip-flop C changes)
Third state →	0	0	0	(flip-flop B changes)
Fourth state →	1	0	0	(flip-flop A changes)

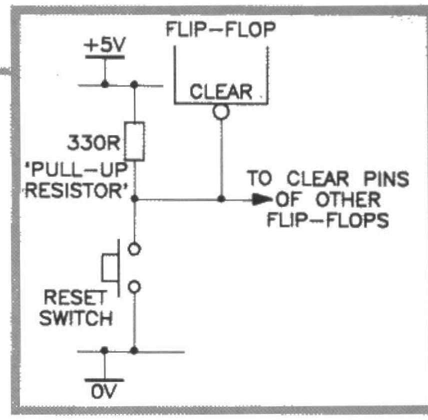


Figure 8. A pull-up resistor speeds up manual set/reset operations.

What does this mean? It means that, in between the two required states, where ABC = 011 and ABC = 100 (going from binary 3 to binary 4, in other words), there are two spurious states: ABC = 010 (2) and ABC = 000 (0). They don't, of course, last very long but they are, nonetheless, there. Since the purpose of a counter is to produce a useful output for one of a number of possible purposes, it means that this output will frequently be in error, unless we can be absolutely sure that the only time that the output of the counter is sampled is when the ripple effect has *finished*. This has to be borne in mind when choosing a suitable counter for a specific application.

On the credit side, the asynchronous counter is fairly simple, saving on component cost, board space, power and so on. It needn't be dismissed out of hand.

The synchronous counter, needless to say, eliminates both of the drawbacks of the asynchronous type. It does so, in many cases, at the cost of greater complexity. The term 'synchronous' implies a co-ordinated action which means, in practical terms, that all flip-flops that have to change between successive counter states are

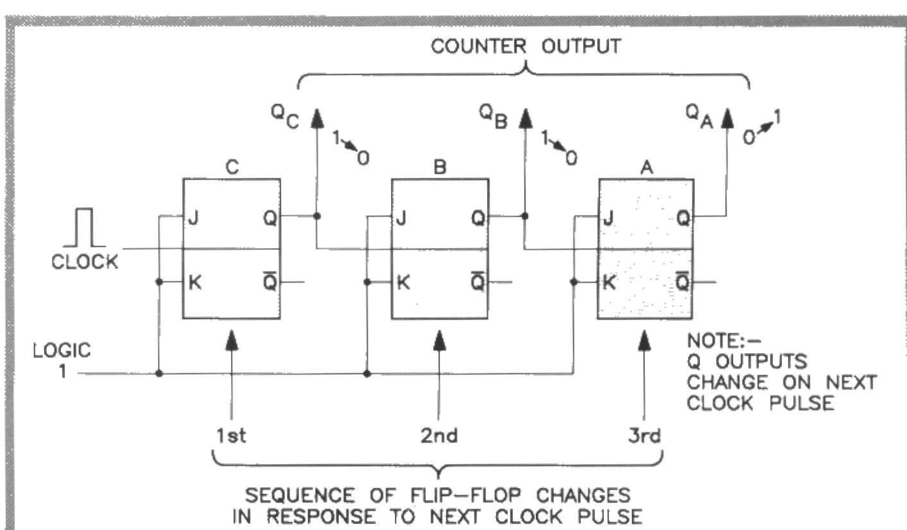


Figure 9. Coding problems in a ripple counter.

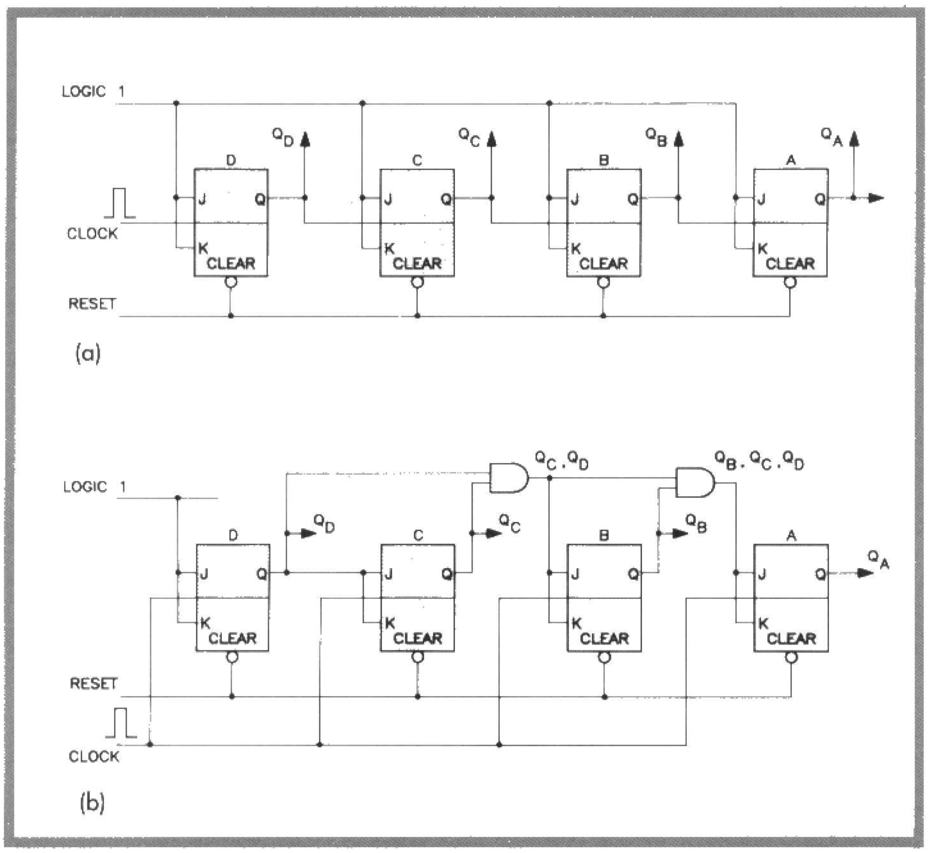


Figure 10. Two 'divide-by-16' binary counters, (a) an asynchronous type and (b) a synchronous version.

forced to do so at *exactly the same time*. This is achieved by clocking them all from a common clock source. Figure 9 shows that only the first flip-flop actually receives the clock pulses; following stages are clocked by the change of level that occurs at the Q output of the previous stage. Although, in the synchronous counter, all flip-flops are clocked simultaneously, those that should not change at any point in the sequence are inhibited from doing so by controlling their J and K steering input levels. An essential part of the design of synchronous counters is concerned with designing the logic to control these inputs.

For comparison, Figure 10 shows two counters that achieve the same end result, a 'divide-by-16' action. The difference is that counter (a) is asynchronous and counter (b) is synchronous. The points made above regarding the extra logic needed for the latter, and the clock connections should be noted.

The previous discussions have laid the groundwork for what follows in the succeeding parts of this series. Those who already have a good working knowledge of counters may have found much of it rather basic. No apology is made for that, certain concepts and conventions have to be acquired at the start. In the next issue we take a look at what is available in terms of the chips themselves and begin to see how to make the best uses of them.

Micro-computer Testing and Fault Finding Part 2 continued from page 63.

The BBC Micro RAM is built up using 4816 devices, each of which offers a capacity of 16K × 1 bit. 16 of these provide 16K × 16 bits, which is configured to provide (32K × 8 =) 32K bytes of RAM. The ROM used in the BBC Micro is a single 23128 chip, which provides (16K × 8 =) 16K bytes. A 2764 8K byte device is also used, configured in a similar way to that of the Einstein.

The 2114 RAM example is straightforward to understand, but in some cases RAM chips will appear to have an insufficient number of address lines (pins). This is because address decoding circuitry is contained within the chip.

A memory chip's size can be found by looking it up in a suitable reference book or component catalogue (such as the Maplin catalogue). In addition, it can be fairly easy to work out the chip's size and organisation from the circuit diagram of the computer in question. Here, the memory size (in bits) can be calculated by multiplying the number of data pins by 2^n, where n is the number of address pins present. For example (with reference once again to Figure 14), the 2114 RAM chip has 10 address pins (A0 – A9 inclusive), which represent an address capacity of (2^{10} =)1024. The number of data pins

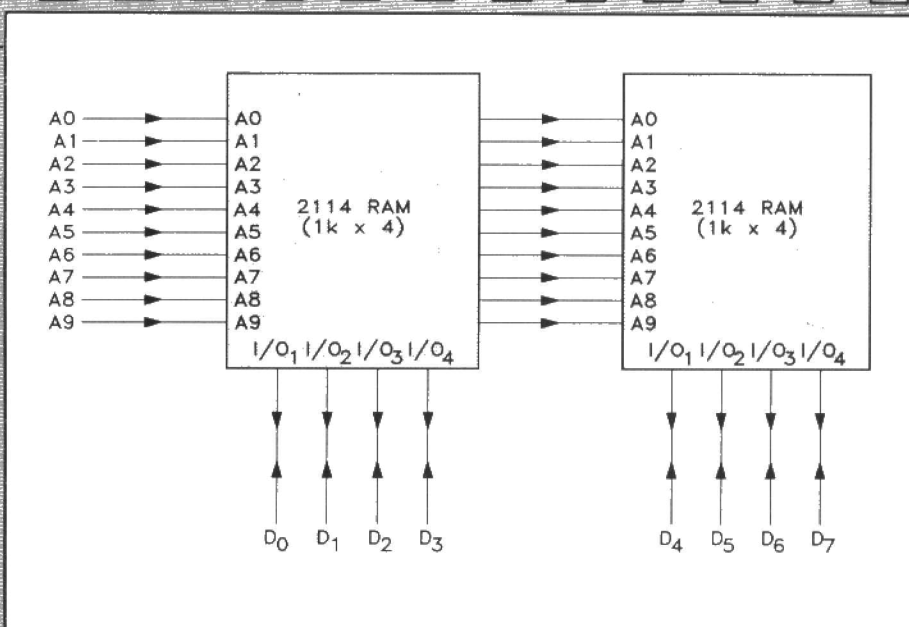


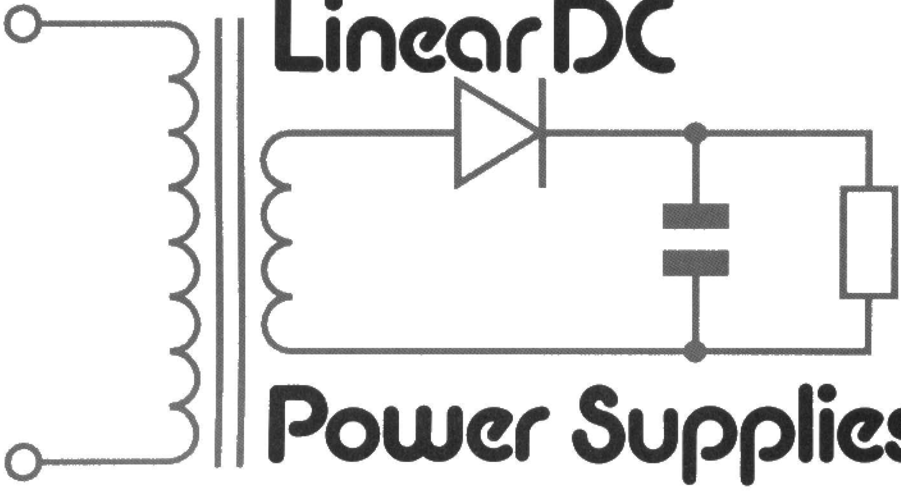
Figure 15. Wiring connections for 1K × 8 memory (2 × 2114).

is 4 (I/O1 to I/O4 inclusive), and thus the memory size is 1024 × 4 bits as already stated.

The Next Stage

In this article we have looked in more detail at input and output circuits and devices, so that those new to microcomputers can begin to make sense from what can sometimes appear to be confusing upon first acquaintance. There is no substitute for actual and detailed experience using appropriate test equipment and techniques, and hopefully this series will encourage intelligent investigation and the ability to carry out at least initial fault-finding tasks. In the next article, we will look at two specific input/output devices; the floppy disc drive and the hard disc drive.

Mains-Operated Linear DC Power Supplies



Part Two – THE REST OF THE BASICS

by J.M. Woodgate B.Sc.(Eng.), C.Eng., M.I.E.E., M.A.E.S., F.Inst.S.C.E.

Update

This is Part 2 of a three-part series, and you will need Part 1 to get the best from this part, so dig out, or order, Issue 48 of the magazine NOW. In Part 1, we looked at half-wave and full-wave (so-called 'biphase half-wave') rectifiers, driven from transformers and followed by capacitive input filters. Some slightly hairy mathematical analysis led to reasonably simple formulae for the transformer secondary voltage and current requirements, and the diode peak and rms currents, in terms of the required load voltage and current. We also noted some general rules, neglect of which is the root cause of many power supply problems.

This time, we are going to look at the full-wave bridge rectifier, voltage doublers and other multipliers, together with direct-on-line supplies, which are directly connected to the mains supply, without a safety isolating transformer. Before we do this, there is one important matter for which there was no space in Part 1.

Diode Voltage Ratings

For the half-wave rectifier, the maximum voltage across the diode occurs when the anode is at the peak of the 'unused' half of the transformer secondary voltage waveform, and is equal to that peak voltage plus the DC output voltage. It is safest to assume that this could be the NO-LOAD DC output voltage, if the circuit develops a fault. The no-load voltage is, in fact, equal to the peak secondary voltage, and we should allow for 10% high mains voltage, so the diode repetitive peak inverse voltage (PIV) rating should be greater than 2·2 times the peak secondary voltage, which is $2{\cdot}2 \times \sqrt{2} = 3{\cdot}1$ times the rms voltage. This means, for example, that the 1N4001 and W005, rated at 50V PIV, can only be used with transformer secondary voltages up to 16V. Since with modern rectifiers, versions with higher PIV (such as 1N4004 and W02) cost hardly any more than those with lower, it is well to be generous with PIV ratings, especially bearing in mind that voltage spikes and jumps occur on the mains supply.

For the biphase half-wave rectifier, the same calculation applies, based on the rms voltage of one half secondary winding.

The Full-Wave Bridge Rectifier

Apart from the biphase half-wave circuit, another way of obtaining the high efficiency of full-wave rectification is the bridge rectifier. This uses four identical diodes (which may be obtained as a single package, such as may be found in Table 14 of the Maplin Catalogue), and a single transformer winding, as shown in Figure 5. During one half-cycle of the secondary voltage, current flows through D1 and D2, while during the other it flows through D3 and D4. The waveforms are exactly as for the biphase half-wave rectifier (Figure 4a in Part 1); in fact the only new formula is that for the rms transformer secondary winding current I_t, which is:

$$I_t = I_l \times (\pi/2p) \times \sqrt{(t_m/t_c)}$$

where I_l is the DC load current; p (which we met in Part 1) is a factor known as the pulse number, the number of capacitor charging pulses per cycle of the supply voltage, and is equal to 2 for all full-wave rectifiers; t_m is the time for one cycle of supply voltage (20ms for 50Hz supplies); and t_c is the duration of a diode current pulse. The rms current I_d through each diode is equal to $I_t/\sqrt{2}$.

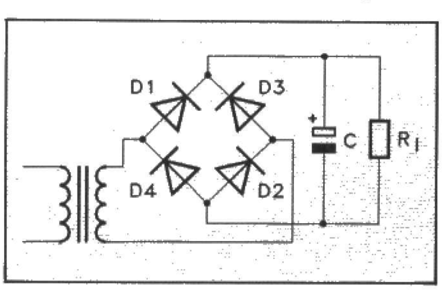


Figure 5. Full-wave bridge rectifier.

The remaining design formulae are the same as we derived for other circuits in Part 1. The open circuit secondary voltage of the transformer is:

$$V_s = (V_l + nV_d)/\{\sqrt{2}\cos(\pi t_c/t_m)\}$$

where V_l is the DC load voltage, V_d is the forward voltage of one diode at the operating temperature, and n is the number of diodes in series, which is normally 2 for a low-voltage bridge rectifier. In this formula, $\pi t_c/t_m$ is in radians: to work in degrees, use $180t_c/t_m$ instead.

The equation connecting t_c/t_m and the resistances R_s and R_l was given in Part 1. R_s is the total resistance in the capacitor charging circuit, and is the sum of R_t, the equivalent resistance of the transformer winding, $2R_d$, the effective resistance of the two diodes in series in each charging path, and R_c, the effective series resistance of the capacitor. R_l is simply the DC load resistance. $R_t = R_2 + n^2R_1$, where R_2 is the DC resistance of the secondary winding, R_1 is the DC resistance of the primary winding and n is the turns ratio, or ratio of the no-load voltages. The equation is difficult to solve for t_c/t_m in terms of R_s/pR_l, but can be solved the other way round, and the results shown as a graph. For convenience this graph, Figure 3, is included in this Part as well as in Part 1.

The peak-to-peak ripple voltage V_r across the capacitor C is given by:

$$V_r = I_l(t_m/p - t_c)/C,$$

and the peak diode current i_{pk} is given by:

$$i_{pk} = I_l(\pi/p)\,(t_m/2t_c)$$

There is no direct current flowing in the transformer secondary winding if the two pairs of diodes are sufficiently nearly identical in forward voltage and resistance, and this is normally easy to achieve.

The PIV rating of the diodes can be determined by noting that, under worst-case conditions, a voltage of 2·2 times the peak secondary voltage appears, as reverse voltage, across two diodes in series, so that each diode has to withstand $1{\cdot}1 \times \sqrt{2} = 1{\cdot}56$ times the rms no-load secondary voltage. This assumes that the reverse voltage divides equally between the two diodes, which is true only if their reverse leakage current/voltage characteristics are identical. Otherwise the diode with higher leakage current takes a smaller share of the voltage. However, for low-voltage supplies, this effect is self-balancing, because only a modest increase in reverse voltage (or temperature) produces a large increase in leakage current, so the division of voltage is always nearly equal. For high-voltage, low-leakage diodes, it may be necessary to connect high-value balancing resistors (e.g. 2·2MΩ), OF ADEQUATE VOLTAGE RATING, in parallel with each diode, so as to prevent the voltage distribution becoming so uneven as to damage one diode.

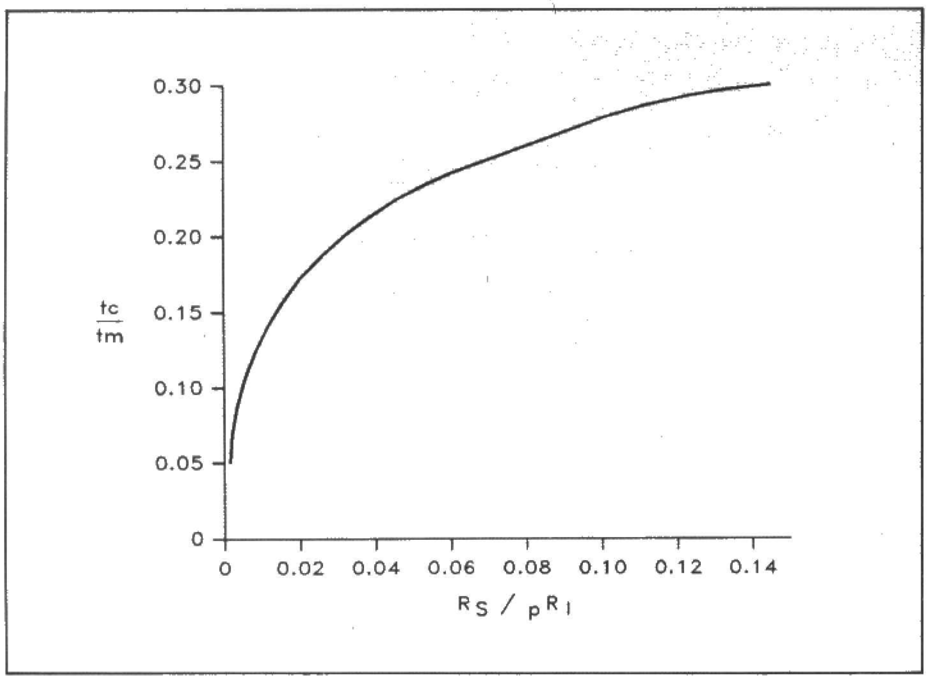


Figure 3. Graph of conduction time/supply period as a function of charging resistance/load resistance (repeated from Part 1).

Experiments

In order to verify the usefulness of the formulae given above and in Part 1, typical power supply circuits (approximately 20V at 600mA DC) were built and very carefully measured. The formulae agreed with the measurements within 2·5% at worst, which is near the limit of accuracy of the methods of measurement used. The least accurate measurement was that of the conduction time t_c, for which a 2-beam oscilloscope display of one cycle of supply voltage and one or two diode current pulses was used. This allows t_c/t_m to be measured directly, but t_c is represented by only about 20mm on the display, so a 2·5% accuracy is all that can be expected. Several of the circuits described below have also been built and measured to verify the information given. It should be emphasised that the formulae are not valid unless the capacitor value is large enough to make the ripple voltage less than about 5% of the DC output voltage.

Voltage Doublers

Quite often, we want a higher voltage than we can conveniently obtain a transformer to provide, especially if we only want a few milliamps of load current. For example, we may have a main 5V 0·5A supply for some logic, but we need a 12V supply at 100mA to produce some external signal at the correct level. We can produce 12V DC from a transformer giving, say 7·5V rms, by means of either of the voltage-doubler circuits shown in Figures 6a, 6b and 6c. The former shows two half-wave rectifier circuits, giving DC outputs of opposite polarity which are connected in series. This circuit, the symmetrical voltage doubler, therefore needs a new formula. The transformer current has no DC component, since the currents from the two halves of the circuit average to zero over one cycle of supply frequency, but the rms value is the rms sum of the currents due to each half-wave rectifier:

$I_t = I_l \times \pi/2 \times \sqrt{(t_m/t_c)}$

The ripple voltages of the two half-wave rectifiers are asymmetrical saw-tooth waveforms which are not 'in step'. The total ripple voltage can be shown (by means of a very complicated diagram and some geometry) to be a symmetrical sawtooth waveform, and the peak-to-peak value V_r is given by:

$V_r = I_l \times (t_m - 2t_c)/C$

If you really want the rms value (which is not much use, despite the number of times it is mentioned in articles), it is $V_r/2\sqrt{3}$.

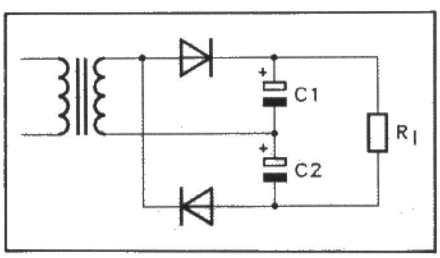


Figure 6a. Symmetrical voltage doubler – half-wave.

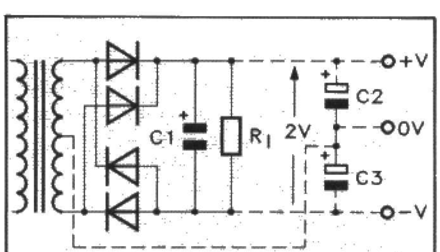


Figure 6b. Is it a doubler? Is it a bridge? It's definitely a full-wave rectifier. For split-rail applications (shown dotted), C1 is replaced by C2 and C3.

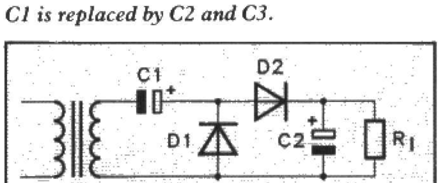


Figure 6c. Diode-pump voltage-doubler.

The Full-Wave 'Doubler'

Figure 6b shows a circuit which can be regarded as either a full-wave version of Figure 6a or as a bridge circuit like Figure 5, simply drawn differently. It isn't really entitled to be described as a doubler, but is clearly a close relative of Figure 6a, which is a doubler. If the transformer winding has a centre tap, as shown dotted, the circuit turns into a simple 'plus and minus rail' supply, ideal for op-amps and audio amplifiers, provided that the 'out-of-balance' current in the 0V rail is reasonably small compared with the currents in the other rails. Note that a packaged bridge rectifier (Table 14 in the Maplin Catalogue) can be used in this circuit, and you only need one, not two. Because it is a bridge rectifier (perhaps with a centre tap), this circuit needs no new formulae *provided that the current in the '0V' rail is small.*

The Diode-Pump Doubler

This circuit is shown in Figure 6c, and is fundamentally different from all the other circuits in many ways. It works as follows. Suppose the bottom end of the transformer winding is initially positive with respect to the top end. C1 then charges through D1, but there is no voltage to drive any current through D2 into C2. On the next half-cycle of supply voltage, the top end of the transformer winding carries the whole charged capacitor C1 positive, and current flows through D2 into C2 and the load resistance. D1 is reverse-biased and passes no current. The DC voltage across C2 is nearly twice that across C1. Note that C1 always has a DC voltage across it, and can therefore be an ordinary electrolytic capacitor. It is best to make the values of C1 and C2 equal. However, the current waveform in D1 is not very close to half a sine wave, so the somewhat simplified theory (Ref. 1) we have been using so far does not give very accurate results. It is best to measure the rms and peak currents, although the same formulae as for the symmetrical doubler do provide a reasonable guide for charging current flow angles between 45° and 65°.

Voltage Multipliers

These circuits are normally used to produce low-current kilovolt supplies from low-voltage mains transformers, and to produce supplies of 50 to several hundred volts from batteries; the latter application is outside the scope of this series. The original Cockroft-Walton multiplier is shown in Figure 7a. This was invented for research into particle physics and widely used, but has a number of drawbacks. Firstly, it is very difficult to analyse the circuit to produce usable design equations, and secondly, the maximum useful number of stages is limited by the ratio of the diode forward voltage to the input voltage. Each stage produces less additional voltage to the extent of one diode voltage, so:

$N_{max} = V_s/V_d$

An alternative circuit was published by Purves and Prescott in 1984 (Ref. 2), and is shown in Figure 7b. Whereas in the Cockroft-Walton circuit the supply voltage

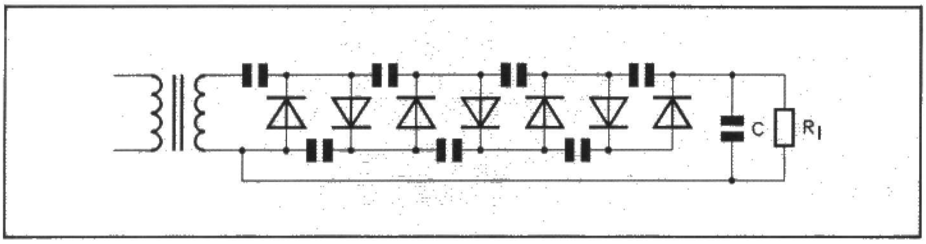


Figure 7a. Cockroft-Walton voltage multiplier. All the capacitor values are different.

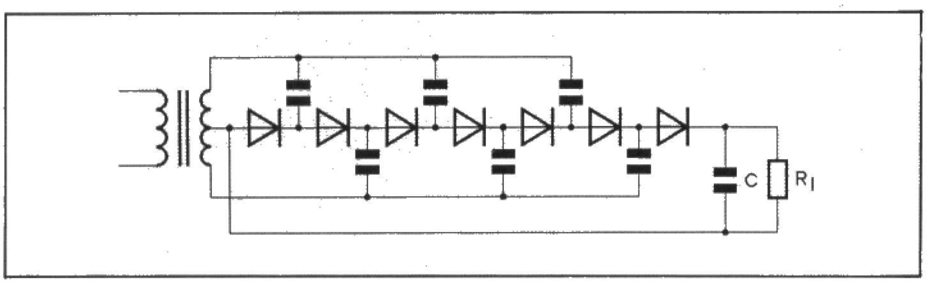


Figure 7b. Purves-Prescott parallel-fed pleoniser, or voltage multiplier. All the capacitor values, except C, should be equal, but the working voltage increases along the chain of diodes.

is applied to one end of the chain of capacitors, in the Purves-Prescott circuit the input is applied to all the capacitors in parallel. For an even number of stages, the waveforms in every stage are identical and design is much easier. Even for an odd number of stages, it is not too difficult, and there is no theoretical limit to the number of stages that can be usefully cascaded. That is not an invitation to try to generate 100kV to see what it looks like! It should be understood that the effective internal resistance of both types of multiplier is proportional to the number of stages and inversely proportional to the supply frequency and the capacitor values. The expression for the internal resistance of the C-W circuit is very complex, but an approximate value for the P-P circuit (supplied from a sinusoidal source) is:

$R_i = \pi/2 \times Nt_m/C$

A More Accurate Analysis

So far, we have mainly been using the analysis (for half- and full-wave circuits) first published by K.L. Smith (Ref. 1), but ths contains a carefully-hidden approximation. It is assumed that the peak of the charging current waveform is time-coincident with the peak of the supply voltage. This, however, is impossible because the charging current starts when the supply voltage exceeds the voltage across the PARTLY DISCHARGED reservoir capacitor but stops when the supply voltage falls below that of the CHARGED capacitor. A glance at Figure 2d or Figure 4b in Part 1 will show this. So the peak of the current waveform actually occurs earlier in the supply cycle than the peak of the supply voltage waveform. This is taken into account in a more accurate and far more complex analysis by A. Lieders (Refs. 3 and 4), where the phase difference between the current and voltage peaks is expressed as an angle δ. Provided that the ripple voltage is within our '5% of DC output voltage' limit, δ is much less than 10° and can be neglected: this is the main simplification adopted by K.L. Smith. Lieders' analysis does not assume that the charging current waveform is a half-sine wave, but incidentally shows that it nearly is, providing V_r is small. Both Smith and Lieders give details of comparisons of theoretical and measured values using their design methods, but these relate to very low power units, of the order of 3W, so are not very useful for general practical applications. This is why I have built and measured most of the circuits.

Direct-On-Line Rectifiers

These circuits are directly connected to the mains supply AND CAN BE LETHAL UNLESS YOU OBSERVE ALL THE NECESSARY SAFETY MEASURES. The reason I have included them here is that they are widely used in electronic controls for lighting and other purposes, so people often come across them. There is, after all, no point in isolating the power supply from the mains if the circuits it feeds are connected to the mains! But this is the only circumstance in which these circuits may be used.

The requirement is usually to produce a DC voltage between 5V and, say, 24V from the mains, without the cost, weight and space involved with a transformer. A rectifier directly connected to the mains supply would produce about 340V DC on no-load, so we have to 'lose' many volts, preferably without generating too much heat.

The Series-Resistor Circuit

For a low-current supply and quite a high DC output voltage, a series resistor is practicable (Figure 8a). The resistor has to pass the diode current, which is greater than the load current but not as high as for the transformer-fed half-wave rectifier. Because in this case R_s is actually larger than R_l, the diode conduction angle is very nearly 180°, and it is convenient to do the design calculations in terms of peak voltages and currents. The peak diode current i_{pk} is given by:

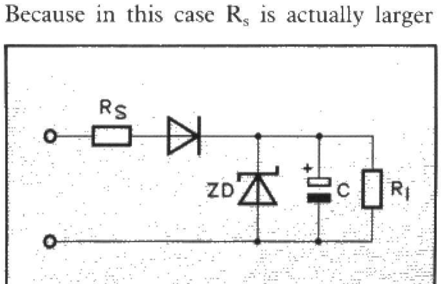


Figure 8a. Direct-on-line rectifier with series resistor.

$i_{pk} = \pi I_l$,

I_l being the total load current including that through the Zener diode. The peak input voltage is $240 \times \sqrt{2} = 339{\cdot}4V$, so that, for a DC supply voltage V_l,

$R_s = (240\sqrt{2} - V_l)/(\pi I_l)$

The rms diode current I_d is $i_{pk}/2$, so the power dissipated in R_s is:

$P = \pi^2 I_l^2 R_s/4$

We can calculate the peak-to-peak ripple voltage V_r by assuming that the voltage across the capacitor C falls linearly as C discharges during the time $(t_m/2)$ of one half cycle of the supply, which is nearly true if the ripple voltage is small:

$CV_r = \Delta Q = I_l t_m/2$,

where ΔQ is the change in charge on C, so:

$V_r = I_l t_m/2C$

The peak inverse voltage (PIV) rating of the diode must exceed the peak voltage of the mains supply plus the DC output voltage, and with a good safety margin to allow for spikes and surges on the supply.

The Series-Capacitor Circuit

The heat produced by the 4W resistor in the above design may be undesirable, and can be eliminated by using a series capacitor to drop the voltage instead. THIS DOES NOT ISOLATE THE CIRCUIT FROM THE MAINS, NOT EVEN IF YOU USE ONE CAPACITOR IN EACH OF THE SUPPLY LEADS. However, the series capacitor, which must be of a type suitable for continuous working at mains voltage (such as JR37S or FA24B), is bigger than a resistor, and more expensive.

The circuit is shown in Figure 8b, and looks like a diode pump voltage doubler.

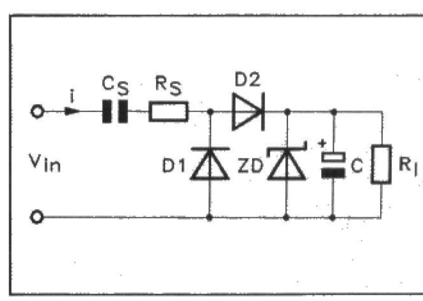


Figure 8b. Direct-on-line rectifier with series capacitor.

However, the large series impedance modifies the situation, and the diode D1 simply provides a return path for the DC load current. Without it, the capacitor simply charges up over the first few cycles of input voltage and the load current then falls to zero. The voltages across the capacitor and the diode D1 are both very nearly sinusoidal, and are 90° out of phase, as shown by the phasor diagram in Figure 8c. Thus the D1 voltage has hardly any effect on the capacitor value required, which depends only on the load current.

Worst-Case Analysis

Since the tolerance on the value of these mains-rated capacitors is often ±20%, and the mains voltage varies from time to time, the design of this circuit is a good introduction to 'worst-case analysis' and 'tolerance engineering'.

In order to keep the working reasonably simple, it will be assumed that the load current does not vary between different versions of the circuit, and that the Zener voltage does not vary with Zener current and between diodes. So we have two tolerances to consider, those of the capacitor value and the mains voltage, and we have to ensure:

- that the Zener current is greater than zero with the smallest capacitor value and the lowest mains voltage, so that the DC output voltage will still be regulated,

and

- that the Zener current is not so high with the largest capacitor value and the highest mains voltage that the power dissipation rating of the diode is exceeded, which would probably cause the diode to fail to short-circuit.

Numerical Example

It will be easier to follow the working if we use some typical figures. Suppose we want a 12V DC supply at 10mA (which could be an awful lot of 4000-series CMOS at a low clock rate!). We take the minimum allowable value of Zener current to be 5mA, and choose QH16S for the Zener. This has a power rating of 500mW at 25°C. The minimum rms mains voltage is 240V − 10% = 216V, and the peak value of this is $216\sqrt{2}$V. The total load current is 15mA, so the peak current is $15\pi \times 10^{-3}$A. The capacitive reactance X_c is thus given by:

$X_c = v_{pk}/i_{pk} = 216\sqrt{2}/(15\pi \times 10^{-3}) = 6482\Omega$

Thus

$C_s = 1/(2\pi f X_c) = 491\text{nF}$

This is the MINIMUM allowable value, so we have to use something larger.

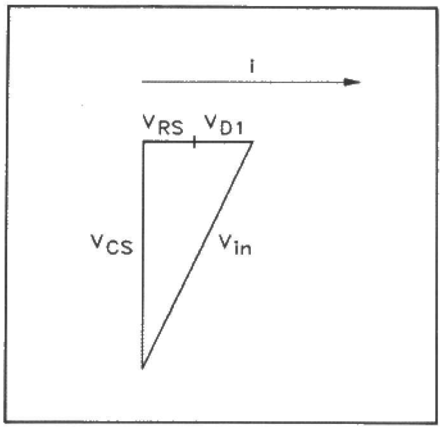


Figure 8c. Phasor diagram for Figure 8b. V_{cs} is very nearly equal to V_{in}.

The minimum value of a 470nF ±20% and a 100nF ±20% in parallel is 456nF, which is too small, so we have to use 470nF (JR36P) and 220nF (JP35N) in parallel, giving a mimimum value of 552nF, and a minimum Zener current higher than our lower limit of 5mA.

If we now look at the upper limits of tolerance, we find an rms mains voltage of 240V + 6, and a capacitance value of 1·2 × (470 + 220) = 828nF. So:

$I_l = i_{pk}/\pi = 240 \times 1{\cdot}06 \times \sqrt{2} \times 2\pi f \times 828 \times 10^{-3}/\pi$

$= 29{\cdot}8\text{mA}$

Of this, 10mA is the useful load current, so the remaining 19·8mA flows through the Zener diode, whose dissipation is thus 19·8 × 12 = 238mW, comfortably less than the 500mW rating and allowing for a considerable rise in local ambient temperature above the 25°C for which the rating is valid.

Switch On – BANG!

We haven't said anything about the resistor R_s in Figure 8c yet, and it is not there for fun. Without R_s, when we switch on the only limit to the inrush current is the resistance of diode D2 and that of the capacitors C and C_s, perhaps 2Ω in all. If we happen to hit the peak of the mains voltage waveform at the instant of closing the switch, the applied voltage is 360V, so the current is 180A! This will bang the diode, and it won't do either capacitor any good either. We have to include R_s to limit this current, and because the repetitive peak current ratings of most silicon rectifier diodes are quite high (10A for the 1N4000 range, for example), it is practicable to limit the current to this value or below, rather than the higher non-repetitive rating, giving a useful safety margin. If we use 1N4005 diodes (PIV = 500V) in this case, the value of R_s must be 360/10 = 36Ω minimum, and, although the power dissipation is only about 80mW, a wirewound or metal film component should be used because of the high current pulses that may occur. It would be better to limit the current to a lower value, by using, say, a 180Ω resistor, whose dissipation would still be only 0·4W.

The formulae for the rms diode current I_d and the ripple voltage V_r are the same as for the series-resistor circuit.

Trailer

Next time, we will have a computer-aided design programme, which works on a different principle to the design equations we have used in Part 1, and this will also allow us to take a useful look at fuses – what current rating to use and what those letters 'T' 'F', and 'HBC' mean, and terms like 'time-delay' as well.

References

1. K.L. Smith, 'DC supplies from AC sources – Part 3', Wireless World, Vol. 91 No. 1588 (Feb. 1985) (Part of a series of six articles published in September and October 1984, February, May, June and October 1985).
2. R.D. Purves and C. Prescott, 'The parallel-fed voltage multiplier', Wireless World, Vol. 90 No. 1578 (March 1984).
3. A. Lieders, 'Single-phase rectifier circuits with CR filters Part 1 – Theory', Electronic Components and Applications, Vol. 1 No. 3 (May 1979).
4. A. Lieders, 'Single-phase rectifier circuits with CR filters Part 2 – Design Procedure', Electronic Components and Applications, Vol. 1 No. 4 (June 1979).

NEXT issue

In next month's super issue of 'Electronics – the Maplin Magazine', there are some really great projects and features for you to get your teeth into! The February issue is on sale 3rd January 1992, available from Maplin's regional stores and newsagents countrywide, and of course by subscription (see page 44 for details). To whet your appetite, here's just a taster of some of the goodies on offer:

THE 386/486 DEBATE

This article discusses these recent Intel devices and the advantages that they will bring to the everyday microcomputer user – and to those with machines somewhat more powerful than your average PC!

WATER DETECTOR

This easy-to-build circuit continues the Funtronics series of projects, which are aimed specifically at the beginner.

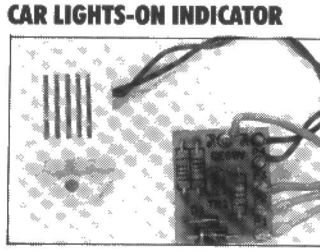
CABLE NEWS NETWORK

A behind-the-scenes look at this American news organisation, which rose to prominence during last year's Gulf War. We also suggest how you may be able to receive this satellite-originated service at home, using existing domestic equipment.

DUAL-RAIL TRACKING VOLTAGE REGULATOR

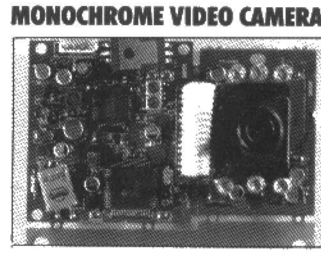
Next month's Data File features the 4195 regulator IC, which greatly simplifies the design of low-current split-rail power supplies.

CAR LIGHTS-ON INDICATOR



A very useful little circuit which sounds a buzzer if your car's lights remain switched on when you leave your car. The low-cost and short time required to fit this device to your vehicle, may save you the inconvenience of a flat battery!

MONOCHROME VIDEO CAMERA



A superb black-and-white camera with a solid-state CCD imager. This reliable sensor is highly sensitive – to both visible and infra-red light, making it an excellent choice for security applications. The unit's compact size is possible due to the extensive use of the latest surface-mounted components.

MICROCOMPUTER TESTING

Disc drives of all types and sizes are covered in the next instalment of Alan Pickard's informative series.

RAISING THE CLANS

by Frank Booty

With the increasing demand for mobile services, technology has provided the market with the Cordless or Cableless Local Area Network (CLAN) to bring mobility to the fixed cabled LAN environment. Indeed there is a very definite trend in the public telecommunications market towards cordless transmission. It has been a proven success in the voice market with the great demand for mobile services, but in the field of data communications, cordless solutions have not always been satisfactory. Figure 1 shows an example of a CLAN.

Only now is the market seeing the advent of Wide Area Networks (WANs) designed specifically for mobile data services. Several organisations (Cognito, Hutchinson and RAM for example) who currently operate mobile data networks are set to lead a significant growth in the transmission of data by mobile users. There are also cordless telecommunications in offices and residential environments. Base stations, from companies such as GPT, are delivering mobility to the PBX as the cellular radio services did for the PSTN. As with the dedicated mobile networks, CLAN technology will bring mobility to the fixed cabled LAN environment.

CLAN APPEAL

CLAN technology represents the convergence of two of telecommunications fastest growing markets: LANs and mobile communications. But on the face of it, it seems unlikely that cordless/cableless/wireless data comms should appeal to users. Hitherto, data comms manufacturers have designed products to promote peace of mind for the user. Suppliers have offered safety, security, reliability and robustness.

Some industry observers argue that CLAN technology seems to offer additional problems in transmitting data – interference, security and a health risk. So does CLAN technology applied to local area networking deliver a benefit to the user, or is it just another example of technology driving the market?

Fixed cabled LANs are undoubtedly a success. Today, the value of the European market is over $1·5 billion and this is expected to grow to over $2·5 billion by 1995 (although you do have to take some predictions with a degree of scepticism). According to comms consultancy, Schema, the UK's market is estimated at $500 million today, growing to $750 million by 1995.

The speed of the technology race is fast. As the LAN market generally is progressing so quickly, there are many other technologies apart from CLANs vying for the network manager's attention. There are fibre optics devices and the FDDI (fibre distributed data interface) ISO network standard, bridging routers, very small aperture terminals (VSATs) and satellite links, and data broadcasting, for example.

It is considered that CLANs will address a niche in the market. In Europe, the value has been estimated at some $20 million for this year growing to $125 million by 1995, this is illustrated in Figure 2. So it doesn't take much to see that the technology is not going to usurp fixed cable LANs. But cable is expensive, inflexible and at times undependable. It is considered that up to 90 per cent of failures in fixed LANs are caused by cabling difficulties. The cost of changing cabling structure or installing additional nodes restricts the users' mobility. To avoid such inconvenience and cost of moving nodes, the LAN has to be planned carefully before it is installed.

In a large installation, this could require a dedicated computer system to manage the miles of cable and the changes to the morphology. All of this could be overcome by using CLAN technology. Despite differences in propagation techniques and portions of the radio spectrum used by CLANs, the hardware components are remarkably similar.

Each network is no more than a network interface card installed in the networked terminals/PCs and an external omnidirectional antenna. At a minimum,

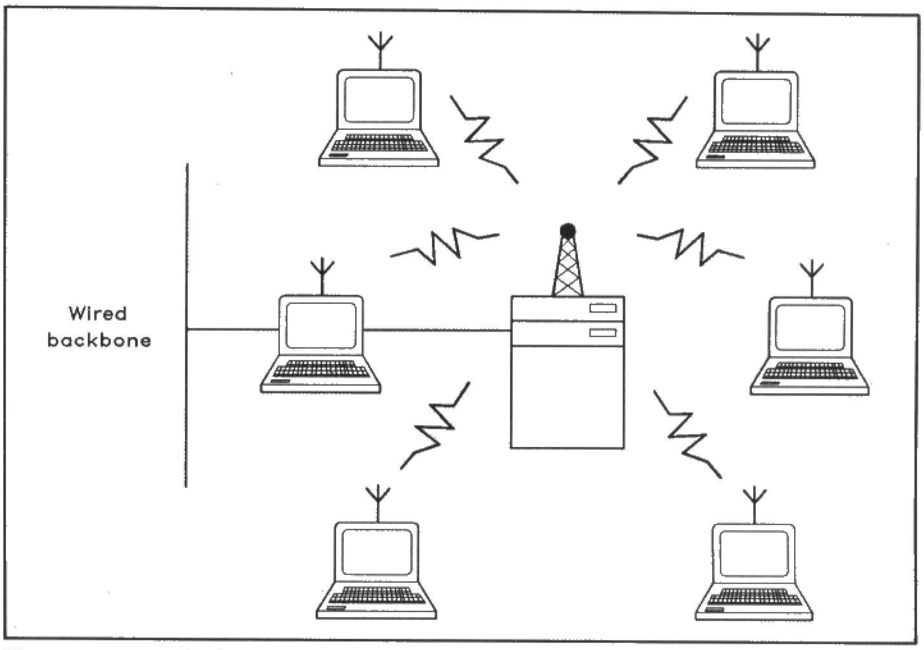


Figure 1. An example of a CLAN.

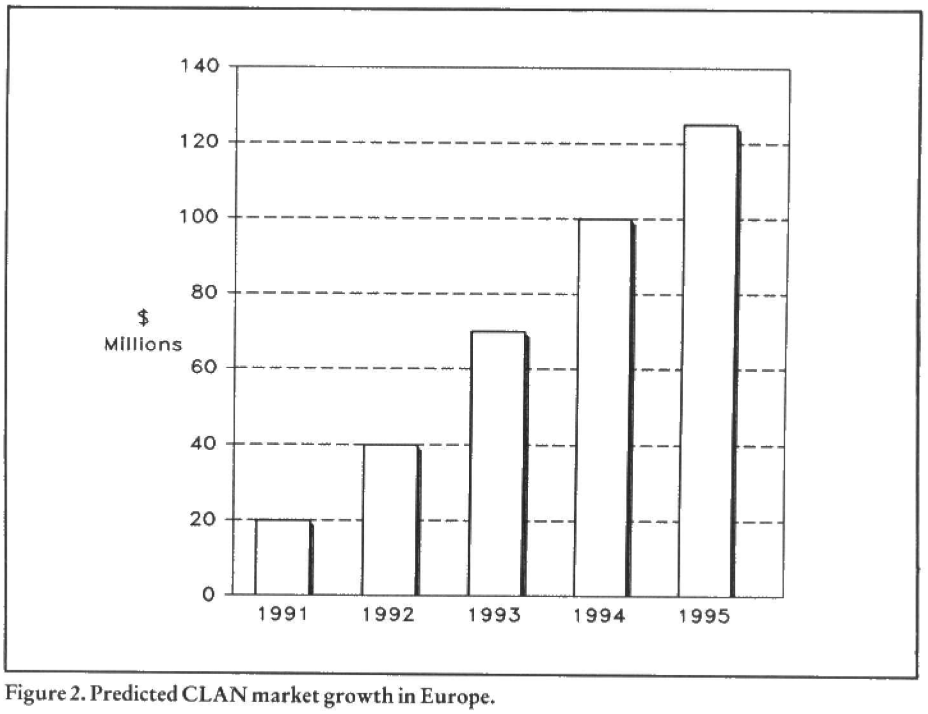


Figure 2. Predicted CLAN market growth in Europe.

the software component of the CLAN would include network drivers, diagnostic software and installation tools, and optional monitoring and diagnostic packages. Other extras include encryption facilities, boot ROM sockets and longer antenna extension cables.

DATA PROPOGATION

Once the components are installed, the CLAN behaves like a Token Ring, Ethernet or ArcNet without the inconvenience of cabling. There are three different propagation technologies being used in the transmission of data over CLANs: spread spectrum technology (SST), infra-red and microwave.

SST

The most popular to date has been SST, which is a technique that was developed in the Second World War. In essence, SST spreads the signal over a broadband at a much lower density than a conventional radio signal. The early SST CLANs in North America operated between 902 to 928MHz, which clashed with the UK cellular operators Cellnet and Vodafone, who already used this frequency band. This led to a wait for CLAN suppliers while the DTI allocated an alternative range, in collaboration with the frequency management committee of CEPT.

In May, the DTI allocated the 2·445 to 2·475GHz band which provides commonality with Holland and Germany. The industry's MPT (Model Product Type) specification for UK CLANs is being finalised, as are the UK licensing requirements.

Manufacturers and products in this sector are: Telesystems of Canada with ARLAN (Advanced Radio LAN) marketed by ChaseCom of London and sold by such resellers as HS Dataline, Frontline and Hawke Systems; California Microwave of the US with Radio Link, marketed by IT Security International of Welwyn Garden City and Telecom Systems of Crawley and sold by such resellers as Rock Technology Systems and Maxim Networks; and NCR with WaveLAN, developed in Europe at Utrecht.

Figure 3 shows the structure of the radio link system and Figure 4 shows possible network topologies.

NCR, whose product operates in the US across frequencies from 902 to

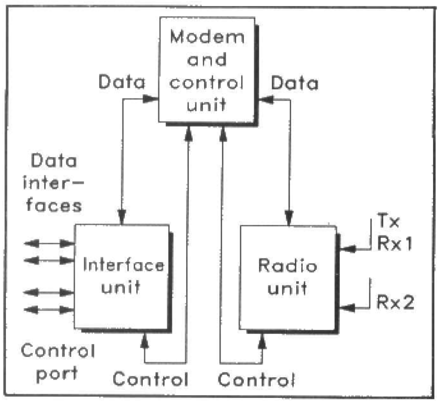


Figure 3. Radio link structure.

926MHz, regards the DTI allocation as fine for the current product offerings but a little light for future product development. NCR believes it will need a greater bandwidth if it is to meet future user requirements and is looking for commonality across the whole of Europe.

Radio Link uses the frequency hopping SST technique as opposed to the direct sequence spectrum spreading technique, which is based on amplitude modulation. Low power levels are used and the frequency hopping sequence is pseudo random, making it virtually impossible to detect and intercept any signals. Figure 5 shows the principle of frequency hopping.

It should be stressed that SST products can be a substitution for cable but are not a replacement for cable. They cannot compete with Token Ring or Ethernet performance, for example.

INFRA-RED

Infra-red propagation is not a means of radio transmission. In fact of the three CLAN technologies, it has the most limitations. But it does have the advantage that its bandwidth is easily re-used. There are major limitations in that it has proven difficult to modulate infra-red propagation for data transmissions, it needs line of sight transmission paths and it cannot penetrate walls.

Consequently infra-red is only applicable in an open office environment. It was also until recently only possible to transmit at 1M bit/s because of the difficulties of modulating the infra-red carrier. BICC Data Networks has now launched InfraLAN which is said to operate at a data rate of 4M bit/s. This is compatible with the IEEE 802.5 standard and provides IBM Token Ring connectivity without any hardware or software modifications to existing equipment.

The company chose infra-red technology because it 'frees end users from concerns about licensing approvals, network security, standards incompatibility or any other issues facing spread spectrum or microwave based cableless systems'. Certainly, DTI licensing is not necessary for users' sites or individual departments. The infra-red signals are also immune from radio frequency interference and are secure from outside signal interception.

BICC has also announced its intention to launch a sister product which would be compatible with IEEE 802.3 Ethernet products.

MICROWAVE

Microwave is the third principal technology suitable for CLANs. A much publicised product here is Motorola's WIN (Wiring Inbuilding Network) system which has gained FCC approval in the US. It transmits at a frequency of 18GHz and is capable of running at 15M bit/s although it is marketed at 10M bit/s (so making it perceived as an Ethernet or Token Ring equivalent). Microwave techniques are less sensitive to physical obstructions and will penetrate through walls although the transmission distance is limited to 100 feet.

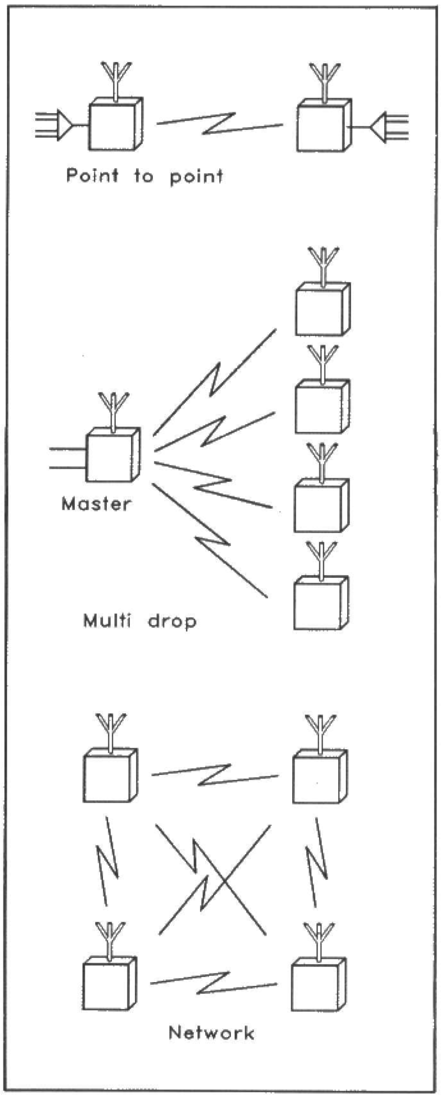


Figure 4. Radio link topologies.

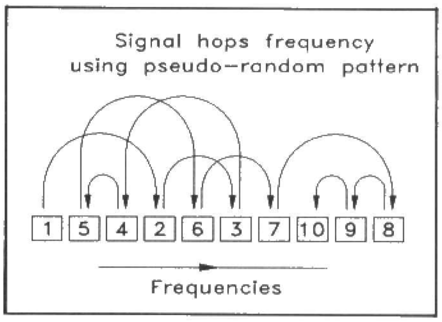


Figure 5. Frequency hopping spread spectrum technique.

To make the WIN system viable several technical hurdles had to be overcome associated with equipment size, expense and the complexity of 18GHz systems. For the UK, Motorola is having to rework the product to enable it to meet DTI specifications and this probably will have happened by the time you read this article.

Microwave has two advantages over both SST and infra-red: there is a lot of spectrum available at these frequencies and the propagation characteristics of 18GHz enable the WIN system to re-use the same frequencies at a range of some 120 feet via a series of deployed microcells in the office environment. However, against this system is the perceived health

risk. While there is no empirical connection between high frequency radiation and health risks, there could well be a serious psychological barrier which would prove insurmountable.

PRACTICALITIES

For all the difficulties experienced by fixed LANs, CLANs is not always or necessarily the perfect answer. CLANs have their own range of operating difficulties: office construction materials disrupt over-the-air transmission between CLAN components to varying extents depending on the propagation method selected; each office has its own topology and each CLAN will have to be set up accordingly – which could mean anything from adjusting an antenna position to moving the server location.

Differences between wavelength availability in different countries decreases the opportunity for volume production and keeps prices high. This is known to concern NCR who are looking for commonality across the whole of Europe – they do not want a different product for each country they market in.

Costs for cable connection to a fixed LAN are declining all the time (it's about £250 to £500 per node). CLAN connection costs are somewhat higher. Using ARLAN, it's about £800 per connection. For Radio Link, one has to spend about £2,500 per box. However, BICC claims that for a structured cabling approach involving 150 IBM Type 1 connectors, one would spend £19,128, 78% of which is in cable and 22% in portable items. For the same system using InfraLAN and four InfraLAN nodes, one would spend £17,608, 100% of which is portable. The company is obviously going for a market in an aggressive manner.

The speed at which data can be transmitted is lower than for a fixed cable due to the limited availability of unused radio spectrum – a point which is obviously seized on by BICC. The faster of the SST CLANs runs at 2M bit/s compared with the 10M bit/s of Ethernet, and the 4/16M bit/s of Token Ring. For many, 2M bit/s may not be fast enough.

Limited spectrum availability means that CLANs have to be regulated, which could have an affect on the market's growth. The area of licensing sites to operate a CLAN is a particular area of deep discussion, with one anticipated outcome being a 'plug in and go' solution without the added complexity of licensing.

Security on CLANs is seen by users as being weaker than it is for a fixed LAN. Using radio suggests the possibility of networks being broken into. In fact, the use of radio in no way compromises the security of the network. SST is the most secure form of CLAN because it is so difficult to decode.

Despite the fact that telecommunications has suffered from being driven by the technology available rather than by user needs, there are situations where CLAN technology could solve real problems. This could be either by extending the usefulness of fixed LANs or in new market opportunities, not necessarily as a substitute product.

APPLICATIONS

The most successful CLAN application to date has been in the retail industry where the Point of Sale (PoS) terminals in large stores have become intelligent terminals that resemble a PC rather than an old fashioned till. Today's PoS terminal requires access to shared applications over a store-wide LAN. But department stores change their layouts to encourage customers to look at different merchandise. So the store management can lose track of the cabling or damage cabling when it is being moved, etc. The work has to be carried out at night or on a Sunday. CLAN technology overcomes all these problems. NCR's WaveLAN product was first piloted in JC Penny's department store in Chicago. Figure 6 illustrates a trial system used to demonstrate CLANS to the Marks & Spencer chain of stores; as a result an order for 500 systems has been placed.

Other applications include:

Networking within listed buildings where internal rewiring is not allowed. Buildings where the ducts are already full to capacity. Buildings where the structure is such that it makes it uneconomical to cable.

Companies with short leases on their premises, making the installation of a fixed LAN uneconomical.

Mobile teams that stay on various sites temporarily, e.g. teams of auditors or management consultants.

Hospitals can take advantage of a flexible data link between nursing stations and patients to keep a constant monitor of the situation.

Manufacturing companies could install flexible computer aided manufacturing and process control, e.g. in hostile environments such as steel mills, hazardous work areas, etc.

As part of an organisation's contingency plan to back up conventional cabling in the event of a disaster.

A LAN could be set up centrally for a company's satellite sites which would save on time and travel costs and a LAN could be installed without the expertise leaving its central location.

Inter-building or network bridges for multiple networks. Also, a CLAN can be connected into a wired backbone offering an even broader flexibility to the user.

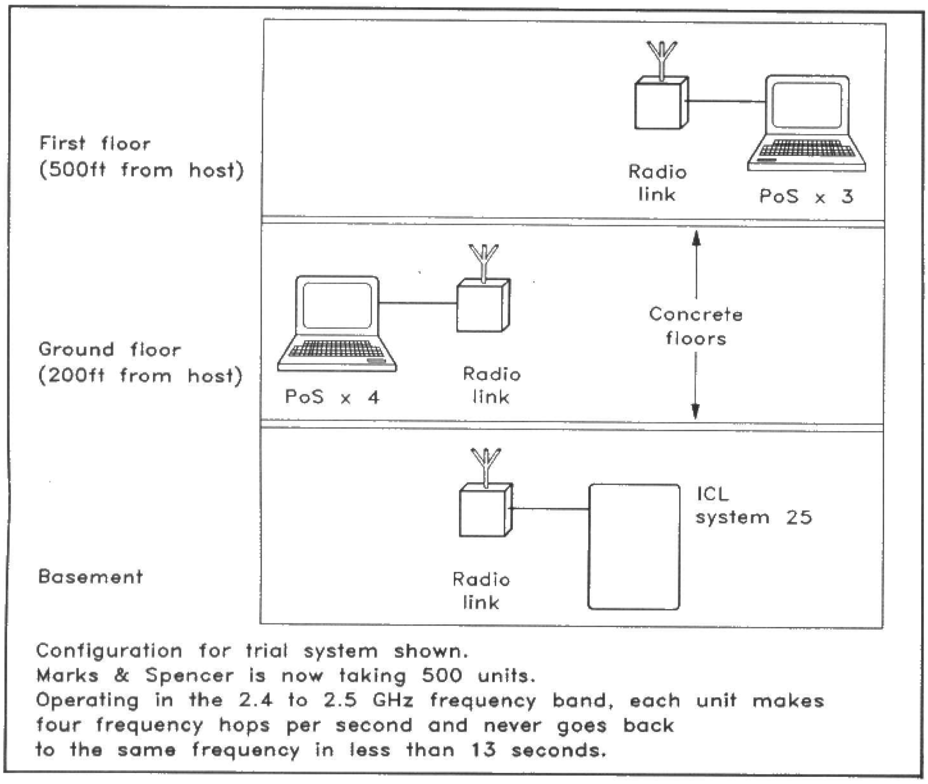


Figure 6. Demonstration radio link system for Marks & Spencer.

CONCLUDING

The key to a successful market is whether it can be cost justified. Given the costs mentioned earlier vis-à-vis CLAN and fixed LAN connections, the trade-off for users will be between speed of transmission against mobility. If there is a chance of moving, then it might be that the CLAN will have paid for itself after the first or second move. The scale of savings that CLANs could make is shown in the US where it is estimated that the cost of cable relocation in 1990 was over $1 billion.

The CLAN market is gaining momentum from the supply side. More suppliers are making themselves known on this side of the Atlantic following their successes in North America. From the users' perspective it is a market where there is a pent-up demand, as it provides a solution for a wide range of problems. The scale of the demand depends on the skilfulness with which these products are marketed, the reliability of the product and ultimately how well it is received by users.

by Dave Goodman

CLEANING UP YOUR ACT

Eric Clapton and I have several things in common – we both play Strat's, love the Blues and are the same age (groan!). Except for the beard, all similarity abruptly stops there. I wonder if he spends his spare time rummaging around back street music shops searching out equipment, inspiration and *free magazines* as I often do? In fact you can get a lot of useful ideas from these freebies, which nicely brings me to the real reason for writing. A recent article, penned by the able hand of a well-known Mr A. Legg, concerned improving the output from dull sounding guitar amplifiers by using a couple of piezo tweeters. He kindly recommended Maplin as a source of further info' on this subject and as we are an obliging lot here in the Lab . . . !

Q "So what's so clever about using piezo electric tweeters?"

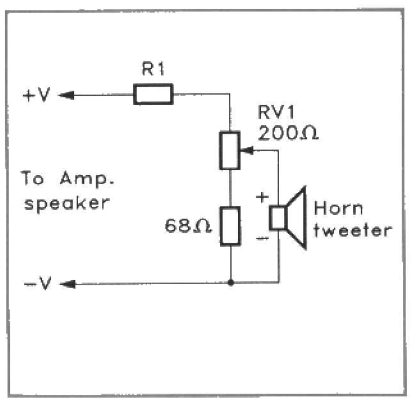
A Basically, piezo crystals 'bend' when a voltage is applied to them. If a small diaphragm is then fixed to the crystal we have the makings of a more conventional speaker. No coils, low dynamic mass, high efficiency and excellent transient response all result in a crisp, clean sound with very low distortion.

Q "OK, that's all very well, but how is it used?"

A Now for the technical stuff. Before letting loose with screwdriver and hammer check that your amp is not under any guarantee as mods are likely to clobber such agreements! Of the several piezo tweeters available from our range, three versions are particularly good for guitar use: The Wide Dispersion Horn, Standard Horn Flushed and Recessed Horn. Generally, guitar amps bash out the power from 50W to 150W (RMS), which will certainly damage these tweeters if they are directly wired in, so resistors (potential dividers) are needed to prevent this from happening. Either one or two tweeters can be used (how's the budget?) and the diagrams show circuit connections for both.

Q "I'm with it so far, but what do I connect the tweeter circuit to?"

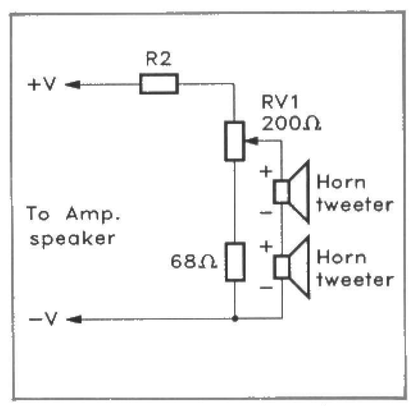
A Directly across the loudspeaker terminals or, if you're lucky, from your amp's EXTension speaker 4 or 8Ω output socket using a mono ¼in. jack plug (the centre terminal is usually +V). The loudspeaker's +V terminal may be coloured red, marked +V, or have a round coloured label stuck next to it for identification.



Single piezo.

Amp Rating	Speaker	R1	R2
50W	8Ω	68Ω	—
	4Ω	10Ω	—
75W	8Ω	120Ω	—
	4Ω	33Ω	—
100W	8Ω	180Ω	10Ω
	4Ω	56Ω	10Ω
150W	8Ω	270Ω	33Ω
	4Ω	120Ω	10Ω
200W	8Ω	330Ω	68Ω
	4Ω	180Ω	10Ω

Table 1. Resistor list.



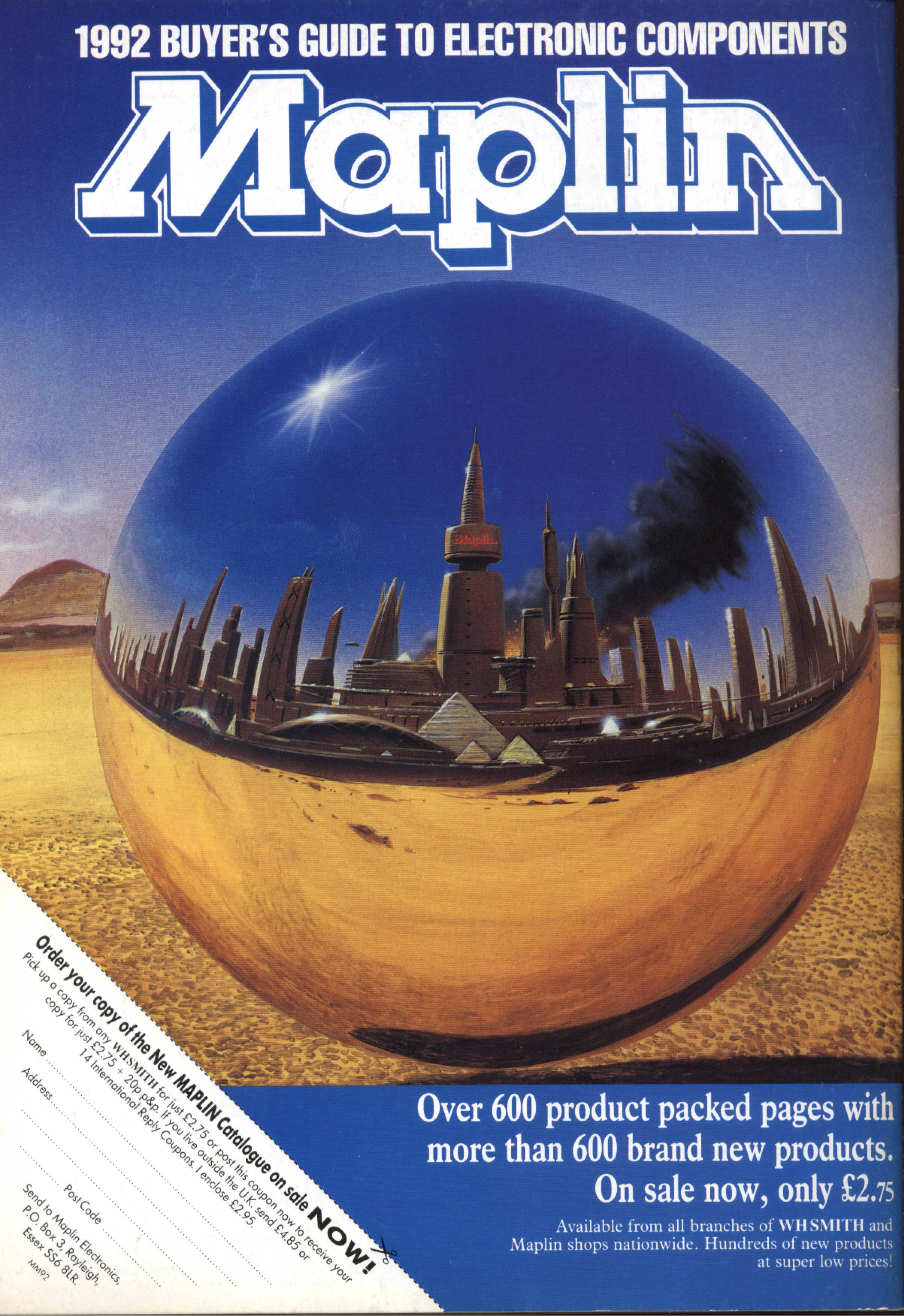
Dual Piezo.

Piezo electric tweeters have a high Sound Pressure Level (100 to 104dB) which means that you don't need to pump the watts into them to get the trebles buzzing. I suggest using our 200Ω speaker volume control which can then be tweaked at will. Good news for all you rhythm and lead 'Mr. Cleans' out there, but not so for the Bassmen. These tweeters are definitely *not* suitable for Bass harmonic enhancement at all!

PARTS LIST

RESISTORS: (3W W/W Min)

10Ω	(W10R)
33Ω	(W33R)
56Ω	(W56R)
68Ω	(W68R)
120Ω	(W120R)
180Ω	(W180R)
270Ω	(W270R)
330Ω	(W330R)
L/S Control 200Ω	(FX99H)
Wide Angle Piezo	(WF56L)
Piezo Horn Flush	(WF09K)
Piezo Horn Recessed	(WF55K)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